PY32T092 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Features

- Core
  - 32-bit ARM® Cortex®-M0+
  - Frequency up to 72 MHz
- Memories
  - 256/192/128/64 KB Flash memory
  - 32/24/16/8 KB SRAM
- Clock management
  - 8/16/24/48/64 MHz High-speed internal RC oscillator (HSI)
  - 2 MHz Medium-speed internal RC oscillator (MSI)
  - 32.768 kHz Low-speed internal RC oscillator (LSI)
  - 4 to 32 MHz High-speed external crystal oscillator (HSE)
  - 32.768 kHz Low-speed external crystal oscillator (LSE)
  - PLL (supports 2 to 18 multiplication of HSI or HSE)
- Power management and reset
  - Operating voltage: 1.8 to 5.5 V
  - Low power modes: Low-power run, Sleep, Low-power sleep, Stop and Standby
  - Power-on/power-down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detector (PVD)
  - V_{BAT} supply for RTC and backup registers
- Input/output (I/O)
  - Up to 60 I/Os, all available as external interrupts
  - All IOs support 50 mA sink current
  - 8 LED COM pins with configurable ultra-strong sink current:
    120/100/80/60 mA
  - 16 GPIOs as LED SEG with constant-current drive
- Touch key
  - High-sensitivity design enables non-contact touch sensing
  - 10 V dynamic CS test-passed anti-interference mode
  - 32 touch channels with derived functions
- 7-channel DMA controller
- 1 x 12-bit ADC
  - Up to 23 external input channels
  - Voltage reference: V_{CC}, internal reference 0.6V/1.024V/1.5V/2.048V/2.5V
  - Input range: 0 to V_{REFP}
- 1 x 12-bit DAC (with 1 channel)
- 2 x comparators
- 1 x operational amplifier
- Support 8 * 36 / 4 * 40 LCD
- 14 timers
  - 1 x 16-bit advanced-control timer (TIM1)
  - 1 x 32-bit general-purpose timer (TIM2)
  - 4 x 16-bit general-purpose timers
  - 1 x PWM dedicated timer
  - 2 x basic timers (TIM6/TIM7)
  - 2 x low power timer (LPTIM)
  - 1 x independent watchdog timer (IWDG)
  - 1 x window watchdog timer (WWDG)
  - 1 x SysTick timer
- RTC
  - Support perpetual calendar
- Communication interfaces
  - 2 x serial peripheral interfaces (SPIs) with I²S function
  - 2 x universal synchronous/asynchronous receiver/transmitters (USARTs), support automatic baud rate detection, ISO7816, LIN and IrDA

  - 2 x universal asynchronous receiver transmitters (UARTs)
  - 2 x low power universal asynchronous receiver/transmitters (LPUARTs)
  - 2 x I^{2}C interfaces support Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz) 7-bit/10-bit addressing, SMBus/PMBus compatible
  - 1 x CANFD interfaces
- Hardware CRC-32 module
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: -40 to 105 ℃
- Packages: LQFP64

Content

1. Introduction

The PY32T092 series incorporate a 32-bit ARM® Cortex®-M0+ core and operates at up to 72 MHz with a wide voltage range. It integrates up to 256 KB Flash and 32 KB SRAM, available in multiple package options. The device integrates multi-channel I²C, SPI, USART, LPUART and other communication peripherals. It has one 12-bit ADC, one DAC, 14 timers, two comparators, one operational amplifier, one CANFD and one LCD driver.

The PY32T092 microcontrollers operate across a temperature range of -40 to 105 °C and a standard voltage range of 1.8 to 5.5 V, provides Low-power run, Sleep, Low-power sleep, Stop0/1/2/3 and Standby low-power operating modes, which can meet different low-power applications.

The PY32T092 series feature excellent touch and control characteristics. Coupled with its outstanding anti-interference performance, it can be adapted to touch buttons and main control in various solutions. Its applications span smart appliances, IoT, wireless communication, gaming devices, industrial controls, and consumer electronics.

Table 1-1 PY32T092 series product features and peripheral counts

Peripherals		**PY32T092R2xT7**
Flash (KB)		256
SRAM (KB)		32
Timers	Advanced control	1 (16-bit)
	General purpose	4 (16-bit)
		1(32-bit)
	Basic	2
	PWM	1
	Low power	2
	SysTick	1
	Watchdog	2
Comm. interfaces	SPI[I^{2}S]	2[2]
	I^{2}C	2
	USART	2
	UART	2
	LPUART	2
	CAN	1
DMA		7ch
RTC		Yes (perpetual calendar)
GPIOs		60
ADC (external + internal)		1 (23+5)
DAC (number of channels)		1(1)
Comparators		2
OPA		1
LCD (COM*SEG)		8*36/4*40
Touch Key		32
Max. CPU frequency		72 MHz
Operating voltage		1.8 to 5.5 V
Operating temperature		- 40 to 105 ℃
Packages		LQFP64

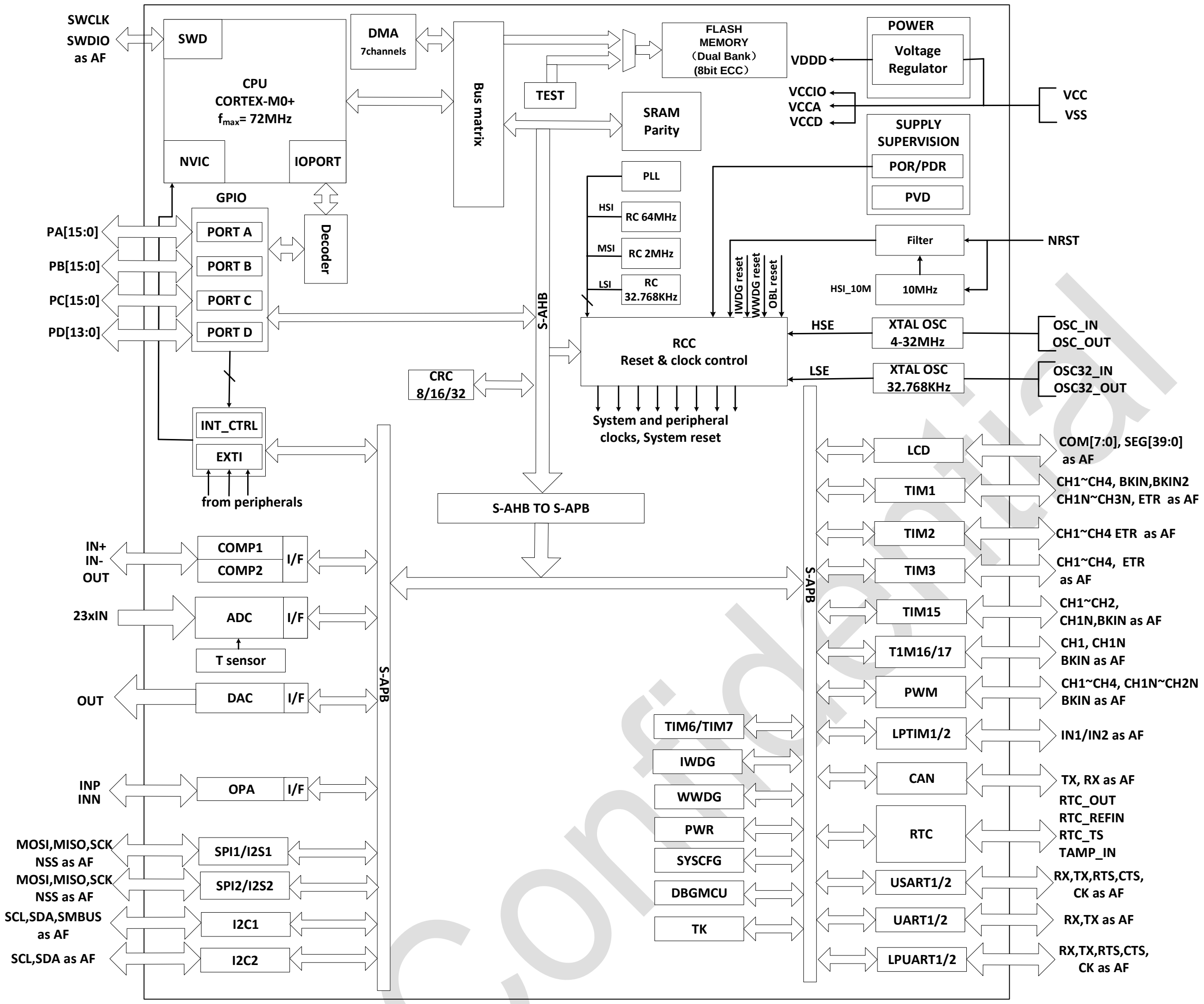


Figure 1-1 System block diagram

2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®-M0+ is an entry-level Arm 32-bit Cortex processor designed for embedded systems. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier. Outperforms 8/16-bit MCUs in code efficiency.

The Arm® Cortex®-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits) and supports write protection and byte parity check.

Embedded Flash, including 8-bit-Flash ECC, contains two different physical areas:

- Main flash area supports dual-bank structure for application/user data
- 8 KB of Information area:
  - User data
  - Parameter bytes
  - Option bytes
  - UID bytes
  - System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 8 KB.
- Option byte write protection is a special design for unlock.
- proprietary code read out protection (PCROP)

The integrated error correction code (ECC) in Flash supports:

- 1-bit error detection and correction
- 2-bit errors detection

2.3. Boot modes

At startup, the BOOT0 pin and boot selector option bit nBOOT are used to select one of the four boot options in the following table:

Table 2-1 Boot mode configuration

BOOT_LOCK	Boot modes		Mode
	nBOOT1 bit	BOOT0 pin	
1	X	X	Forced Boot from Main flash
0	X	0	Boot from Main flash
0	1	1	Boot from System memory
0	0	1	Boot from SRAM

The Boot loader is located in the System memory and is used to reprogram the Flash memory by using USART.

2.4. Flash accelerator (ACC)

In order to utilize the full performance of the processor, the gas pedal will implement instruction prefetch queuing and branch caching, thus increasing the speed of program execution in Flash. According to CoreMark benchmarks, the performance obtained by this gas pedal needs to reach the equivalent of Flash executing the program with wait cycles at CPU frequencies up to 72 MHz.

- Command prefetch
- The instruction cache supports 32 branch entries with a 64-bit data bus width
- The data cache supports 2 branches with a 64-bit data bus width

2.5. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- An 8/16/24/48/64 MHz internal high-precision configurable HSI clock
- A 2 MHz internal high-precision MSI clock
- A 32.768 kHz configurable LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock, and used to enable the CSS function to detect LSE. If CSS fails, the hardware will automatically convert the system clock to LSI, and software configures the LSI frequency. Simultaneously, CPU NMI interrupt is generated.
- PLL clock has HSE or HSI source. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 72 MHz.

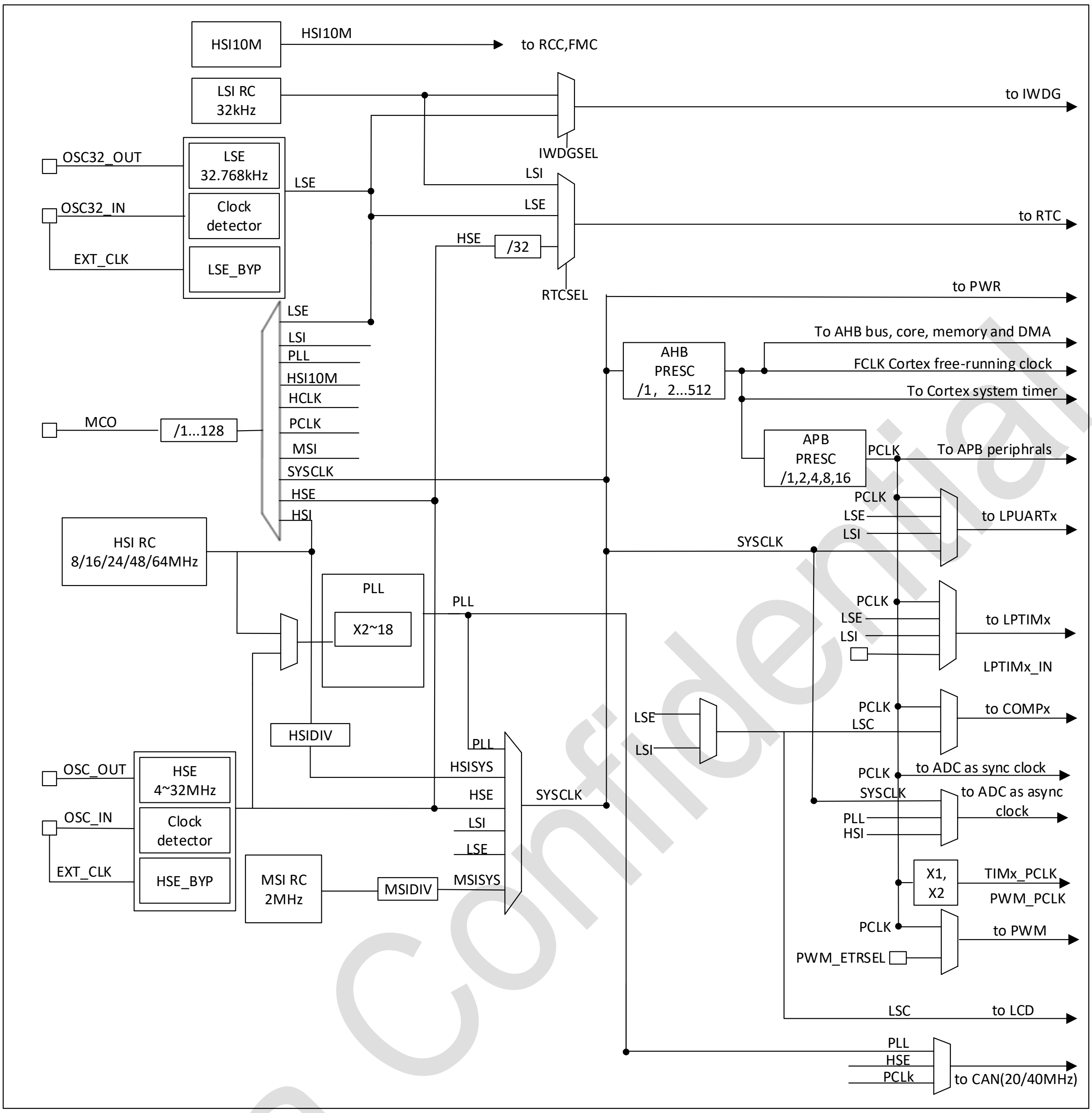


Figure 2-1 System clock structure diagram

2.6. Power management

2.6.1. Power block diagram

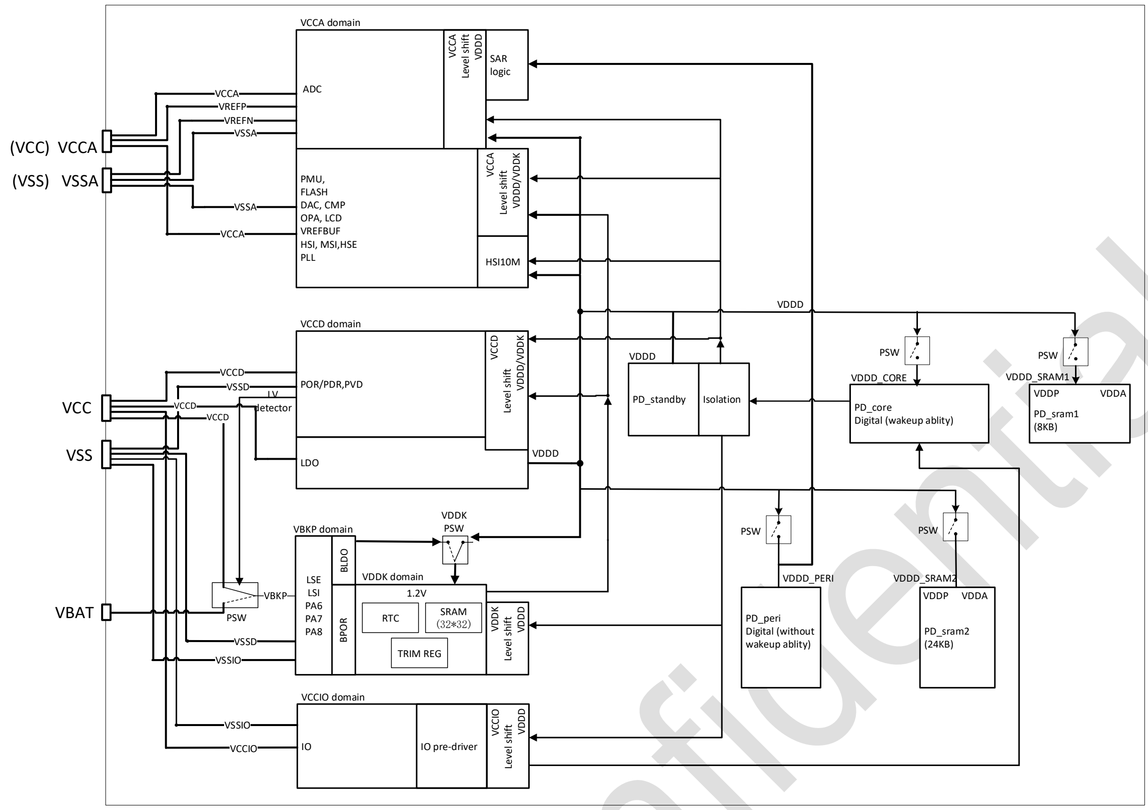


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Value	Descriptions
1	V_{CC}	1.8 to 5.5 V	The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits
2	V_{BAT}	1.55 to 5.5 V	Power supply. When V_{CC} is powered down, the V_{BKP} domain is powered by V_{BAT}.
3	V_{CCA}	1.8 to 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
4	V_{REFP}	1.8 to 5.5 V	Reference voltage for ADC and DAC
5	V_{DD}	1.2 V	VR supplies power to the main logic circuits (CPU, bus, RCC, PWR and peripheral IPs) and SRAM inside the device. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the Stop or Standby mode it powered by MR, LPR and DLPR.

2.6.2. Power monitoring

2.6.2.1. Power-on reset/power-down reset(POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed to provide power-on and power-down reset for the device. The module keeps working in all modes.

2.6.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte and both the rising and falling detection points can be individually configured.

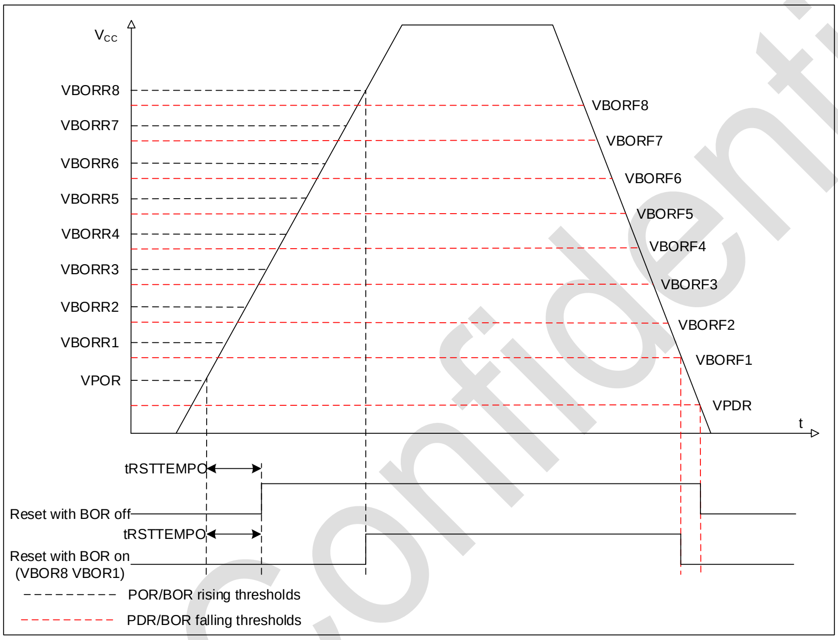


Figure 2-3 POR/PDR/BOR threshold

2.6.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

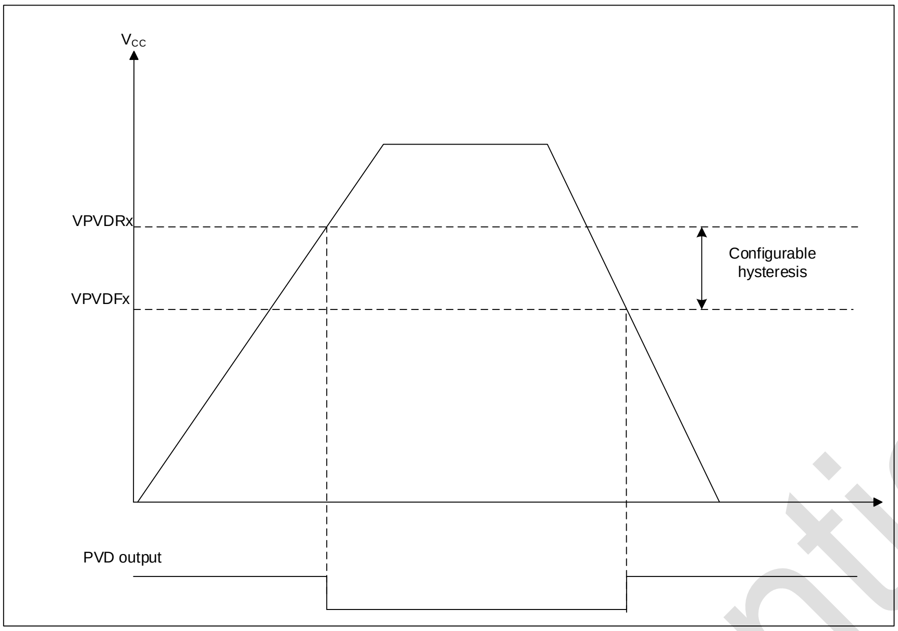


Figure 2-4 PVD threshold

2.6.3. Voltage regulator

The regulator has three operating modes:

- Main regulator (MR) is used in Run mode.
- Low power regulator (LPR) provides an option for even lower power consumption in low power mode.
- Deep low power regulator (DLPR) ensures the lowest power consumption in low power mode.

2.6.4. Low-power mode

In addition to the normal operating mode, there are five low-power modes:

- Sleep mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the essential modules, and power them down immediately after use.
- Low-power run mode: The Max. CPU frequency is 2 MHz and the voltage regulator operates in low-power mode to save energy.
- Low-power sleep mode: entered only from Low-power run mode and CPU core clock is turned off. The system returns to Low-power run mode when awakened by an event or interrupt.
- Stop0/Stop1/Stop2/Stop3 modes: SRAM and register contents are retained. Clocks (PLL, HSI, MSI, HSE) and most module clocks in the V_{DDD} domain are disabled. Specific modules can be configured to power down. Wake-up sources: GPIO, PVD, COMP, LPUART, I^{2}C, IWDG, TK, RTC, TAMP and LPTIM.
- Standby mode: partial digital logic and SRAM in the V_{DDD} domain are powered down. Four exit conditions: External reset via NRST, IWDG reset, RTC alarm wakeup, and valid edge on the WKUP pin.

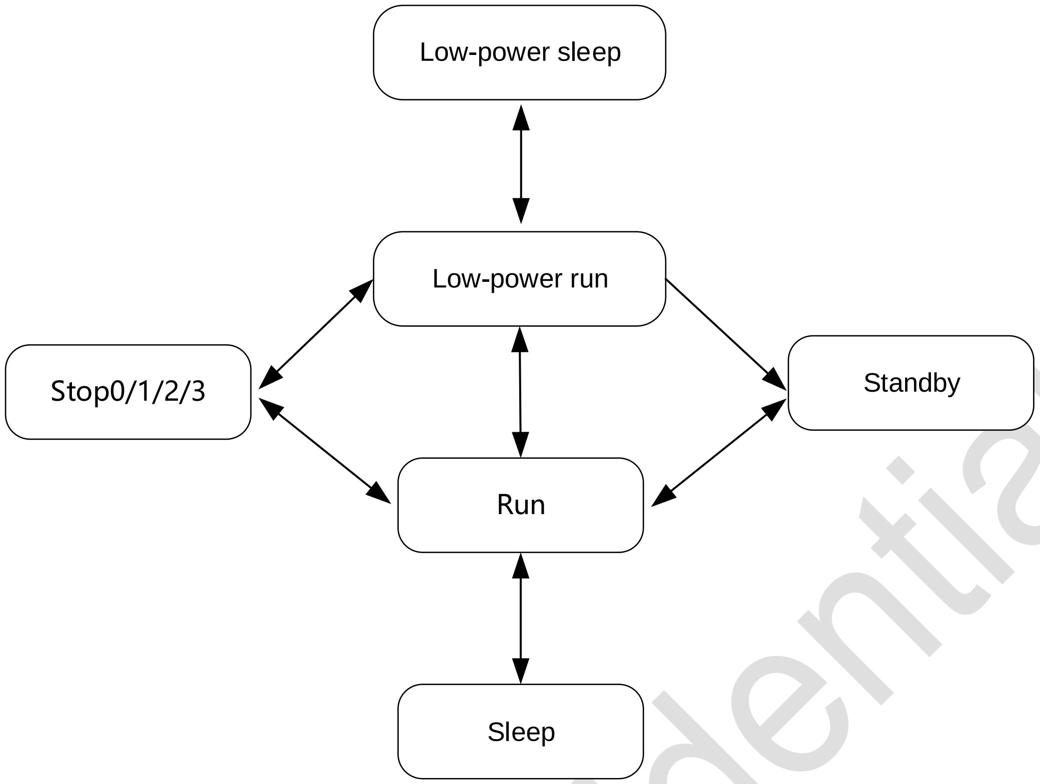


Figure 2-5 Power consumption state transition diagram

2.7. Reset

Two resets are designed in the device: power reset and system reset.

2.7.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.7.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)

2.8. General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. GPIO features are summarized as follows:

- Support read/write operations via IO Port or AHB bus
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)

- Speed selection for each I/O
- Input states: floating, pull-up/down, and analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers (Max. 16 alternate functions for each IO)
- Fast toggle capable of changing every clock cycles
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions

2.9. Direct memory access controller (DMA)

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The DMA controller have 7 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 7 configurable channels
- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between multiple requests on the same DMA module is software-programmable. For equal priorities, hardware resolves conflicts (lower channel number = higher priority).
- The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. Source and destination addresses must be aligned to the transfer width.
- Programmable address modes: Increment, decrement, or fixed
- 4 event flags: transfer complete (circular mode), block transfer, half-block transfer and transfer error,ogically ORed together in a single interrupt request for each channel
- Support transfers between memory to memory, peripheral to memory, memory to peripheral and peripheral to peripheral
- SRAM, APB and AHB peripherals can act as source or destination. Flash can only act as a source.
- Support single-trigger mode and four circular modes:
  - Peripheral address retained, memory address retained
  - Peripheral address reloaded, memory address retained
  - Peripheral address retained, memory address reloaded
  - Both addresses reloaded
- Single-trigger mode: Programmable transfer count (0 to 65,535)
- Circular mode: Infinite looping or finite looping (1 to 255 cycles)
- Support single transfer and bulk transfer
  - Single transfer: Generates 1 ACK per data transfer

  - Bulk transfer: Generates 1 ACK after all configured data is transferred (bus released post-completion).
- Two transfer modes
  - Fast mode: Holds the bus until all data is transferred
  - Round-robin mode: Releases the bus after each transfer for re-arbitration
- Support pausing transfers upon entering the block transfer Complete interrupt in circular mode.

2.10. Interrupts and events

The PY32T092 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.10.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle non-maskable interrupts (NMI) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 32 maskable external interrupts
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.10.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events by GPIO and modules (PVD, COMP, RTC, TAMP, I^2C, LPUART, TK and LPTIM).

The EXTI controller has multiple channels, including up to 60 GPIOs multiplexed using 16 EXTI lines, one PVD output, two COMP outputs, two LPUART signals, two I^2C, two LPTIM wake-up signals, TK, RTC, TAMP and LSE CSS signal. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.

- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.11. Analog-to-digital converter (ADC)

The PY32T092 has a 12-bit SARADC. The module has a total of up to 30 channels to be measured, including 23 external and 5 internal channels, including 3 pairs of differential channels.

The internal channels are： T_{S_VIN}, V_{REFINT}, $V_{CC}/3$, OPA and DAC.

- A/D conversion of the various channels can be performed in single, continuous, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- Interrupt generation at ADC ready, the end of sampling, the end of conversion, end of sequence conversion, analog watchdog or overrun events
- The ADC is configurable with 12/10/8/6-bit resolutions.
- Maximum ADC sampling rate: 2 MSPS
- Support self-calibration (initiated by software)
- Support programmable sampling time
- The data register allows configurable data alignment
- Support DMA requests for regular channel data conversion
- Support configurable conversion of 16 regular channels
- Support configurable conversion of 4 injected sequences
- The oversampler is equipped with a 16-bit data register. The oversampling rate can be adjusted from 2 to 256, and the programmable data shift can reach up to 8 bits.
- Data processing supports gain compensation and offset compensation.

2.12. Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The DAC can be configured in 8-bit or 12-bit mode, or can be used in conjunction with a DMA controller. When the DAC is operating in 12-bit mode, the data can be left justified or right justified. The DAC module has one output channel The main features are as follows:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA support for each channel
- Support DMA underflow error detection
- External triggers for conversion
- Input reference voltages: V_{CC}, V_{REFP}, and V_{REFBUF}
  — The V_{REFBUF} of the DAC only supports 2.5 V

2.13. Comparators (COMP)

The PY32T092 integrates two general-purpose comparators (COMP), namely COMP1 and COMP2. The COMP1/2 module can be used as a separate module or in combination with timer.

The COMP features:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer
- Voltage comparison function is supported. Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - 64 steps voltage of V_{CC}/V_{REFBUF}
  - Temperature sensor output
  - DAC output
  - OPA output
  - V_{REFINT}
- Programmable speed and power consumption
- Programmable hysteresis function
- Write protection for configuration registers (LOCK function)
- The output can be triggered by a connection to the I/O or timer input
- Each COMP has interrupt generation capability and is used to wake up the device from low power mode (Sleep/Stop) (via EXTI)
- Provide software to configure the digital filtering time to enhance the anti-interference capability of the device
- Support output blanking to reduce switching noise
- Support the window comp function

2.14. Operational amplifier (OPA)

The OPA module can be flexibly configured and is suitable for simple amplifiers.

OPA features are summarized as follows:

- One independently configured operational amplifier
- The inputs can be individually configured to select from two channels, and the outputs can be configured to select from four IO channels. The outputs can be internally directed to the comparator and ADC.
- The input range of the OPA is from 0 to V_{CC}, and the output range is from 0.2 V to V_{CC}-0.2 V.
- Can be configured for the following models
  - General purpose OPA

2.15. Liquid crystal display controller (LCD)

The liquid crystal display (LCD) controller is a digital controller/driver for monochrome passive LCD, with up to 8 common terminals (COM) and 40 segment terminals (SEG) to drive 160 (4 * 40) or 288 (8 * 36) LCD pixels. The exact number of terminals depends on the device pins described in the data manual. LCD functions are summarized as follows:

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6, and 1/8 duty cycle
- Support 1/2, 1/3 and 1/4 bias voltage
- Supported display modes: Type A or Type B
- Three ways to generate driving waveforms: internal resistor voltage division, external resistor voltage division, and external capacitor voltage division
  - With internal resistor voltage division, power consumption can be reduced by using software to configure the conduction time of the internal high-drive voltage-dividing resistors, thus matching the capacitance charge required by the LCD panel. The contrast of the LCD can also be configured via software to adjust the brightness of the LCD panel
  - For external resistor voltage division, the capacitance charge required by the LCD panel can be matched by adjusting the resistance value of the external resistors
  - In the case of external capacitor voltage division, the capacitance charge required by the LCD panel can be matched by using software to configure the number of capacitor driving times
- Support LCD flashing function and configuration of multiple flicker frequency configuration
- Support the configurable LCD dead time function to adjust the display brightness
- Unused LCD segments and public pin can be configured to digital or analog functions
- Up to 16 registers LCD data RAM
- Dual buffer memory allows the data in the LCD_RAM registers to be updated at any time through the application firmware without affecting the integrity of the displayed data
- Support low power modes: The LCD controller can perform display operations in Run, Low-power run, Sleep, Low-power sleep, and Stop modes
- Configurable frame interrupt

2.16. Touch key

The PY32T092 integrates a 32 channel capacitive touch circuit:

- Optional internal/external CMOD capacitor, no external capacitor needed for internal use
- High-sensitivity for non-contact touch
- 10 V dynamic CS test-passed anti-interference mode
- Support the frequency hopping function
- Support the waterproof compensation function
- Support multi-channel parallel connection
- In touch mode, the overall power consumption of the device can be less than 13 μA (in Stop3 mode)

2.17. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Timer type	**Timers**	**Counter resolution**	**Counter type**	**Prescaler**	**DMA**	**Capture/compare channels**	**Complementary outputs**
Advance control	TIM1	16-bit	up, down up/down	1 - 65536	Yes	4	3
General purpose	TIM2	32-bit	up, down up/down	1 - 65536	Yes	4	-
	TIM3	16-bit	up, down up/down	1 - 65536	Yes	4	-
	TIM15	16-bit	up	1 - 65536	Yes	2	1
	TIM16,TIM17	16-bit	up	1 - 65536	Yes	1	1
Basic	TIM6	32-bit	up	1 - 65536	Yes	-	-
	TIM7	16-bit	up	1 - 65536	Yes	-	-
Dedicated timers	PWM	16-bit	up, down up/down	1 - 65536	Yes	4	2

2.17.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output
- Support incremental (quadrature) encoders and Hall sensor circuits for positioning.

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 to 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.17.2. General-purpose timers

2.17.2.1. TIM2/TIM3

The general-purpose timers TIM2/TIM3 are consist of 32/16-bit auto-reload counters and a 32/16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the timer link.

- Support DMA function
- The counter can be frozen in debug mode.

2.17.2.2. TIM15/TIM16/TIM17

- The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM15 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM output.
- TIM15/TIM16/TIM17 have complementary outputs with dead time.
- TIM15/TIM16/TIM17 support DMA function.
- The counter can be frozen in debug mode.

2.17.3. Basic timers (TIM6/TIM7)

- The basic timer TIM6 is consist of a 32-bit auto-reload upcounter driven by their programmable prescaler respectively.
- The basic timer TIM7 is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- 16-bit / 32-bit auto-reload upcounter
- Generate interrupt/DMA request on update event (counter overflow).

2.17.4. PWM dedicated timer

This module can generate a pulse width modulation (PWM) signal with a frequency and duty cycle determined by registers. Support external clock counting, and the frequency can exceed the PCLK frequency.

- A 16-bit up, down, or up/down auto-reload counter
- A programmable prescaler that allows the clock frequency of the counter to be divided from 1 to 65,536
- Support write protection for important registers
- Up to 4 independent channels
- Support complementary outputs with programmable dead time for 2 channels.
- Support 1 brake input
- Support DMA function

2.17.5. Low power timer (LPTIM)

LPTIM1/LPTIM2 are 32-bit/16-bit timers. The ability of LPTIM to wake the system from low-power modes makes it suitable for practical low-power applications. LPTIM introduces a flexible clock scheme that can provide the required functionality and performance while minimizing power consumption.

- LPTIM1 is a 32-bit and LPTIM2 is a 16-bit up-counter
- It has a 3-bit prescaler with 8 possible division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Optional clocks include LSE, LSI and APB clock,
- Support single-shot and continuous modes
- Support software/hardware input triggering

- The counter can be frozen in debug mode

2.17.6. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the device, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by LSI or LSE and can work in Stop and Standby mode.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode and Standby mode by reset.
- The counter can be frozen in debug mode.

2.17.7. System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.17.8. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.18. Real-time clock (RTC)

The real-time clock (RTC) is an independent timer that provides an automatic wake-up unit for managing all low-power modes. It is an independent binary-coded decimal (BCD) timer/counter, offering a calendar clock/calendar with programmable alarm interrupt functionality. As long as the power supply voltage remains within the operating range, the RTC will continue to operate regardless of the device's state (run mode, low-power mode, or in reset).The RTC can work in V_{BAT} mode.

The calendar includes subseconds, seconds, minutes, hours (12 or 24 format), day week day, date, month and year, presented in BCD format

- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms
- Allow in runtime correction of 1 to 32,767 RTC clock pulses for synchronization with the main clock.
- Supports reference clock detection: enable the use of a more accurate secondary clock source (50 or 60 Hz) to enhance calendar accuracy
- Equipped with a digital calibration circuit having a resolution of 0.95 ppm to compensate for quartz crystal oscillator errors.

- Time stamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- Comes with a 17-bit auto-reload wake-up timer (WUT) for periodic events, with programmable resolution and period.
- The following three RTC clock sources can be selected:
  - HSE clock divided by 32
  - LSE clock
  - LSI clock
- Three dedicated maskable interrupts:
  - Alarm interrupt
  - Timestamp interrupt
  - Wake-up timer interrupt

2.19. Cyclic redundancy check calculation unit (CRC)

CRC computing unit is based on a fixed generation polynomial to obtain CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- When writing to this register, it serves as an input register, allowing you to input new data for CRC calculation
- When reading from this register, it returns the result of the previous CRC calculation
- Each time data is written to the register, the calculation result is a combination of the previous CRC calculation result and the new one (CRC calculation is performed on the entire 32-bit word rather than byte by byte)
- You can reset the register CRC_DR to 0xFFFFFFFF by setting the RESET bit in the register CRC_CR. This operation does not affect the data in the register CRC_IDR
- Support configuration of the initial CRC value
- Support configuration of the CRC polynomial
- Support inverting the input data in units of 8/16/32 bits
- Support output inversion
- The input data bit width supports 8/16/32 bits.
- The polynomial bit width can be configured as 7/8/16/32 bits, which is equivalent to the bit width of the output data

2.20. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- Enable and disable IO filter
- Enable and disable I^2C Fast mode plus
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- Analog input channel enable
- Enable analog PAD2
- Enable and disable Noise filter for all GPIOs

- Enable and disable PVD Lock
- Enable and disable Cortex-M0+ LOCKUP
- Enable and disable ECC Lock
- Enable and disable SRAM parity check
- LED IO control

2.21. Debug support (DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep, Stop and Standby mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Block I^{2}C1 and I^{2}C2 SMBUS timeouts when the CPU is in HALT mode
- Block CANFD timeouts when the CPU is in HALT mode

The MCUDBG register also provides device ID encoding. This ID encoding can be accessed by a SW debug interface, or by a user program.

2.22. Inter-integrated circuit interface (I^{2}C)

The I^{2}C bus interface handles communications between the microcontroller and the serial I^{2}C bus. It provides multimaster capability, and controls all I^{2}C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

I^{2}C features:

- Two I^{2}C interface
- Multimaster capability: can be master or slave
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast mode (Fm): up to 400 kHz
  - Fast mode plus (Fm+): up to 1 MHz
- As Master
  - Generate clock
  - Generate start and stop
- As Slave
  - Programmable I^{2}C address detection
  - Dual-address capability that responds to two secondary addresses
  - Discovery of the STOP bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^{2}C busy flag bit
- Error flag
  - Master arbitration loss

  - ACK failure after address/data transfer
  - Start/stop error
  - Overrun/underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Hardware packet error checking (PEC) generation and verification with ACK control
- Support SMBus
- Support low-power modes, wakes up from Stop mode on address matching.

2.23. Universal synchronous/asynchronous receiver transmitter (USART)

PY32T092 contains 2 USARTs and supports ISO7816, LIN and IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable STOP bits (0.5, 1, 1.5 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit

  - Check the received data byte
- Configurable Tx and Rx pin SWAP
- MSB First data transmission and reception format
- Support LIN master transmit sync break and slave detect break
  - Generates 13-bit break and detects 10/11-bit breaks when configured for LIN
- IRDA SIR encoder/decoder
  - Support a 3/16-bit duration in normal mode
- Smart card emulation function
  - Smart card interface supports ISO7816-3 asynchronous protocol
  - 0.5 and 1.5 STOP bits for the smart card
  - Configurable MSB or LSB transmission
  - The NACK signal width can be configured to 1/1.5/2 ETU
  - Support transmission error retransmit
  - Support an EGT setting from 0 to 256 and multiple timeout interrupts
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.24. Universal asynchronous receivers/transmitter (UART)

The PY32T092 features two universal asynchronous receivers/transmitters (UARTs):

- Support 5/6/7/8/9-bit serial data
- Support 1/2 STOP bits (1/1.5 STOP bits for 5-bit data)
- Support sending address/data
- Support fixed parity check
- Support break frames
- Detect start bit errors
- Support programmable fractional baud rates
- Support Tx/Rx pin swapping
- Support MSB FIRST endianness switching
- Full-duplex asynchronous communication
- NRZ standard format

- Support DMA transmission
- Support 4-bit fractional baud

2.25. Low-power universal asynchronous receivers/transmitters (LPUART)

The PY32T092 integrates two LPUARTs, supporting wake-up from Sleep and Stop modes.

Features:

- Full-duplex asynchronous communication
- NRZ standard format
- Programmable baud rate
- 32.768 kHz clock with baud rate range 300 to 9600 baud, higher rates need higher clock frequency
- Dual clock domains: PCLK and dedicated kernel clock
- Programmable data word length (7/8/9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable STOP bits (1/2 STOP bits)
- Single-wire half-duplex communications
- Support continuous DMA transfer
- Independent enable for transmission and reception
- Independent polarity control for Tx/Rx signals
- Interchangeable Tx/Rx pins
- Support hardware RS-485/modem flow control
- Parity control: generates parity bit on transmission, checks on reception
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Interrupt sourcrs with flags:
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
  - Match address byte
- Support 5/6/7/8/9-bit serial data
- Support wake-up from Stop, Sleep, Low-power run, and Low-power sleep modes

2.26. Serial peripheral interface (SPI)

The PY32T092 contains two SPI/I^{2}S module.

SPIs allow the device to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (without bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 Master mode baud rate prescalers (Max f_{PCLK}/2)
- Slave mode frequency (Max f_{PCLK}/2)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Support Motorola mode and TI mode
- Master mode fault, overrun flags with interrupt capability
- CRC Error flag
- Two embedded Rx and Tx FIFOs with DMA capability, depth of four, and width of 16 bits (8 bits when data frame is set to 8 bits)

I^{2}S features:

- Half-duplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)
- Data format may be 16-bit, 24-bit or 32-bit
- Packet frame is fixed to 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame) by audio channel
- Programmable clock polarity (steady state)
- Underrun flag in slave transmission mode, overrun flag in reception mode (master and slave) and frame error flag in reception and transmitter mode (slave only)
- 16-bit register for transmission and reception with one data register for both channel sides
- Support I^{2}S protocols:
  - — I^{2}S Phillps standard

  - MSB-justified standard (left-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)
- Data direction is always MSB first
- DMA capability for transmission and reception
- Master clock may be output to drive an external audio component. Ratio is fixed at 256 × f_S (where f_S is the audio sampling frequency)

2.27. CANFD

The PY32T092 contains one CANFD communication interface module.

The CAN module complies with ISO 11898-1: 2015 (CAN protocol specification version 2.0 Part A, B) and CAN with Flexible Data-Rate Specification Version 1.0.

The 0.8 KB message RAM memory enables the Rx filters, Rx FIFO, Rx Buffer, Tx Event FIFO and Tx Buffer functions.

- Applies ISO 11898-1:2015 standard
- Supports Transmitting and receiving up to 64 data bytes
- Supports CAN error logging
- Supports AUTOSAR and SAE J1939
- Supports receive filtering
- two configurable receive FIFOs
- Individual signaling indication when a high priority message is received
- Up to 3 dedicated receive buffers
- Up to 3 dedicated transmit buffers
- Configurable transmit FIFO or queue
- Configurable transmit event FIFOs
- Host CPU has direct access to message RAM
- Supports programmable loopback test modes
- Supports maskable module interrupts
- Two clock domains: the CAN core kernel clock and the APB bus interface
- Supports debugging

2.28. Serial wire debug (SWD)

An ARM SWD interface allows serial wire debugging tools to be connected to the PY32T092.

3. Pinouts and pin descriptions

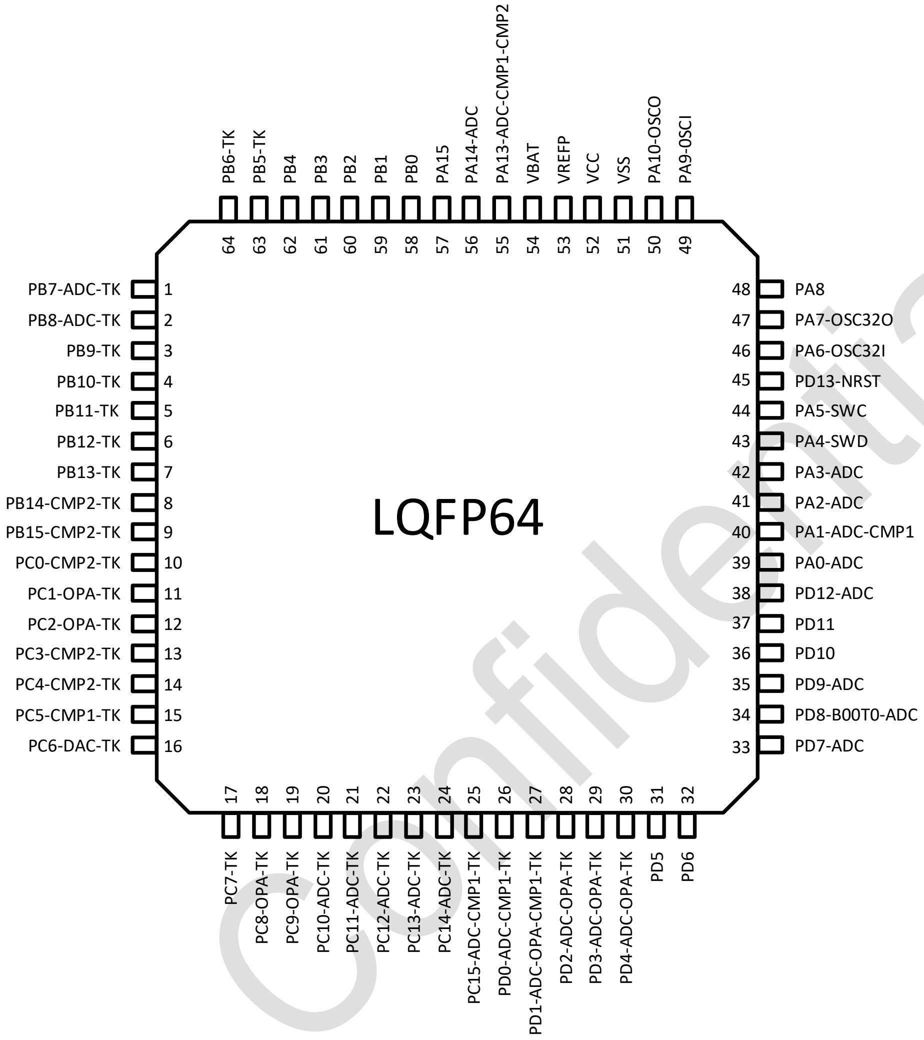


Figure 3-1 LQFP64 Pinout2 PY32T092R2xT7 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I	Input-only pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, with Analog switch function
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
		COM _L	LED COM port supports 120 mA sink current and analog input/output functions
		COM _C	LED SEG port supports constant-current drive and analog input/output functions
		COM _F	I^{2}C Fm+ with analog input function
		COM _T	Tolerant port, allowing input voltage range greater than V_{CC}
		COM _FT	I^{2}C Fm + with analog input capability and Tolerant port capability
Notes		-	Unless otherwise specified, all ports are used as floating inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

3.1. Pin definitions

Table 3-2Pin definitions

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
39	PA0(7)	I/O	COM	USART2_TX TIM1_CH3 LPTIM1_OUT_IN1 COMP2_OUT	ADC0
40	PA1	I/O	COM	TIM1_CH4 TIM1_CH3N TIM3_ETR TIM16_BRK LPTIM2_OUT_IN1 WKUP4	ADC1 COMP1_INM1
41	PA2	I/O	COM	SPI1_NSS/I2S1_WS TIM15_CH2 TIM15_CH1_ETR TIM15_BRK	ADC2
42	PA3	I/O	COM	SPI1_SCK/I2S1_CK TIM2_CH1_ETR	ADC3
43	PA4-SWDIO(2) (3)	I/O	COM_T	DEBUG-SWD	-

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				IR_OUT	
44	PA5-SWCLK(2) (3)	I/O	COM_T	DEBUG-SWC WKUP5	-
45	PD13-NRST(1)	I/O	NRST	USART1_CK TIM2_CH3	-
46	PA6(5)(6)	I/O	COM	USART1_TX USART1_CTS TIM1_BRK TIM2_CH4 TIM15_CH1 EVENTOUT	OSC32_IN
47	PA7(5)(6)	I/O	COM	TIM1_CH1 EVENTOUT	OSC32_OUT
48	PA8(5)(6)	I/O	COM	RTC_OUT/TAMPIN	-
49	PA9	I/O	COM	USART1_RX USART1_TX TIM15_ETR TIM15_CH1 EVENTOUT	OSC_IN

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
50	PA10	I/O	COM	USART1_RX	OSC_OUT
				USART1_TX	
				TIM15_CH2	
51	V_{SS}	G	-	Ground	
52	V_{CC}	S	-	-	
53	V_{REFP}(6)	S	-	-	
54	V_{BAT}	S	-	-	
55	PA13	I/O	COM_F	USART1_RTS	ADC19 COM0 COMP1_INM7 COMP2_INM0
				I2C1_SCL	
				I2C2_SCL	
				TIM1_BRK	
				PWM_CH1	
				EVENTOUT	
				WKUP6	
56	PA14	I/O	COM_F	USART2_RX	ADC20 COM1
				USART2_CTS	
				I2C1_SDA	
				I2C2_SDA	
				TIM15_CH1	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				PWM_CH1N COMP2_OUT MCO EVENTOUT	
57	PA15	I/O	COM_F	USART2_TX USART2_RTS UART1_TX UART1_RX I2C1_SMBA TIM15_CH2 TIM16_CH1 PWM_CH3	COM2
58	PB0	I/O	COM_F	TIM16_CH1N USART2_CK UART1_TX UART1_RX I2C2_SMBA SPI2_NSS/I2S_WS PWM_CH3	COM3

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				PWM_CH4 EVENTOUT PVD_OUT	
59	PB1	I/O	COM	SPI2_SCK/I2S2_CK TIM2_CH3 TIM2_CH1_ETR TIM16_BRK PWM_CH4 EVENTOUT	COM4/SEG36
60	PB2	I/O	COM_L COM_C	SPI2_MISO/I2S2_MCK LPUART1_TX TIM15_ETR LPTIM1_OUT_IN1 EVENTOUT	COM5/ SEG37
61	PB3	I/O	COM_L COM_C	SPI2_NSS/I2S_WS SPI2_MOSI/I2S2_SD LPUART1_TX TIM2_CH2 LPTIM2_OUT	COM6/SEG38

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				**Alternate functions**	**Additional functions**
				LPTIM2_IN1 EVENTOUT	
62	PB4	I/O	COM_F COM_L COM_C	SPI2_SCK/I2S2_CK I2C1_SCL I2C2_SCL TIM1_BRK TIM2_CH3 EVENTOUT WKUP7	COM7/SEG39
63	PB5(SWCLK)(3) (4)	I/O	COM_F COM_L COM_C	SPI2_MOSI/I2S2_SD UART1_RX I2C1_SDA I2C2_SDA TIM2_CH4 DEBUG-SWC	SEG0 TK0
64	PB6(SWDIO)(3) (4)	I/O	COM_L COM_C	SPI2_MISO/I2S2_MCK UART1_TX TIM1_CH3 TIM2_ETR	SEG1 TK1

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				EVENTOUT	
				DEBUG-SWD	
1	PB7	I/O	COM_L COM_C	SPI1_MISO/I2S_MCK	ADC4 SEG2 TK2
				SPI1_NSS/I2S_WS	
				TIM1_CH4	
				TIM1_ETR	
				EVENTOUT	
2	PB8	I/O	COM_F COM_L COM_C	SPI1_MOSI/I2S1_SD	ADC5 SEG3 TK3
				USART2_CTS	
				UART1_RX	
				LPUART1_RX	
				I2C1_SDA	
				I2C2_SDA	
				TIM1_CH4	
				TIM2_ETR	
				EVENTOUT	
3	PB9	I/O	COM_F COM_L COM_C	SPI1_SCK/I2S1_CK	SEG4 TK4
				USART1_TX	
				USART2_RTS	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				UART1_TX LPUART1_TX I2C2_SCL TIM1_BRK TIM2_CH4 PWM_BRK LPTIM1_ETR IR_OUT COMP1_OUT MCO	
4	PB10	I/O	COM_C	SPI1_NSS/I2S1_WS TIM2_CH1 TIM15_CH1_ETR LPTIM2_IN2 EVENTOUT WKUP0	SEG5 TK5
5	PB11	I/O	COM_C	SPI2_NSS/I2S2_WS USART1_RX LPUART1_CTS	SEG6 TK6

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				TIM2_CH1_ETR	
6	PB12	I/O	COM_F COM_C	SPI1_MISO/I2S1_MCK	SEG7 TK7
				SPI2_SCK/I2S2_CK	
				USART1_TX	
				USART2_TX	
				LPUART1_RTS_DE	
				I2C1_SCL/I2C1_SDA	
				I2C2_SCL/I2C2_SDA	
				TIM17_CH1	
				LPTIM1_ETR	
				TIM1_CH1	
7	PB13	I/O	COM_F COM_C	SPI1_MOSI/I2S1_SD	SEG8 TK8
				SPI2_MOSI/SPI2_SD	
				USART2_RX	
				UART1_RX/UART2_RX	
				LPUART1_RX	
				I2C1_SCL/I2C1_SDA	
				I2C2_SCL/I2C2_SDA	
				TIM1_CH1N	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				TIM17_CH1 LPTIM1_ETR MCO EVENTOUT	
8	PB14	I/O	COM_C	SPI2_MISO/I2S2_MCK USART2_TX UART1_TX/UART2_TX LPUART1_TX TIM1_CH1 TIM17_BRK RTC_REFIN LPTIM2_IN2 EVENTOUT	SEG9 COMP2_INP2 TK9
9	PB15	I/O	COM_C	SPI2_NSS/I2S2_WS USART2_CK TIM2_CH1_ETR TIM3_CH3 EVENTOUT	SEG10 COMP2_INM1 TK10
10	PC0	I/O	COM_C	USART2_TX	SEG11

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				TIM2_CH3 TIM3_CH4 TIM15_CH1_ETR PWM_BRK EVENTOUT	COMP2_INM7 TK11
11	PC1	I/O	COM_C	SPI1_NSS/I2S1_WS USART2_CTS CAN_RX PWM_CH1	SEG12 OPA_INM2 TK12
12	PC2	I/O	COM	SPI1_SCK/I2S1_CK SPI2_MISO/I2S2_MCK TIM15_CH1N TIM16_BRK CAN_TX PWM_CH1N	SEG13 OPA_INP2 TK13
13	PC3	I/O	COM	SPI1_MISO/I2S1_MCK SPI2_NSS/I2S2_WS USART1_CTS UART1_TX/UART2_TX	SEG14 COMP2_INP3 TK14

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				**Alternate functions**	**Additional functions**
				UART1_RX/UART2_RX	
				TIM1_CH4	
				TIM16_CH1N	
				PWM_CH2N	
				TIM15_CH1	
				LPTIM1_IN2	
				LPTIM2_OUT_IN1	
14	PC4	I/O	COM	SPI1_MOSI/I2S1_SD	SEG15 COMP2_INP4 TK15
				SPI2_SCK/I2S2_CK	
				USART1_RTS	
				UART1_TX/UART2_TX	
				UART1_RX/UART2_RX	
				TIM1_CH3N	
				TIM16_CH1	
				PWM_ETR_HS	
				LPTIM1_IN2	
				LPTIM1_OUT_IN1	
15	PC5	I/O	COM_F	SPI3_SCK/I2S2_CK	SEG16 COMP1_INM0
				USART1_CTS	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				LPUART1_TX	TK16
				LPUART1_RX	
				I2C1_SCL	
				I2C2_SCL	
				TIM1_CH3	
				TIM1_ETR	
				WKUP1	
				LPTIM1_IN1	
				EVENTOUT	
16	PC6	I/O	COM_F	SPI2_MOSI/I2S2_SD	SEG17 DAC_OUT TK17
				LPUART1_TX	
				LPUART1_RX	
				LPUART2_RX	
				USART1_RTS	
				UART2_RX	
				I2C1_SCL/I2C1_SDA	
				I2C2_SCL/I2C2_SDA	
				TIM1_CH3N	
				TIM3_CH4	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				LPTIM1_OUT_IN1	
				EVENTOUT	
17	PC7	I/O	COM_F	SPI2_MISO/I2S2_MCK	SEG18 TK18
				USART2_TX	
				UART2_TX	
				LPUART1_TX	
				LPUART2_TX	
				I2C1_SDA	
				I2C2_SDA	
				TIM15_ETR	
				TIM16_CH1N	
				EVENTOUT	
18	PC8	I/O	COM	SPI1_MISO/I2S1_MCK	SEG19 OPA_OUT3 TK19
				USART1_RX	
				USART1_TX	
				UART1_RX	
				TIM1_BRK	
				TIM15_CH2	
				LPTIM2_OUT_IN1	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				CAN_RX EVENTOUT	
19	PC9	I/O	COM_F	SPI1_MOSI/I2S1_SD USART1_RX USART1_TX USART2_CK UART1_TX I2C1_SDA I2C2_SDA TIM15_CH1 TIM15_ETR LPTIM2_ETR CAN_TX EVENTOUT	SEG20 OPA_OUT4 TK20
20	PC10	I/O	COM_F	SPI1_SCK/I2S1_CK USART2_RX USART2_TX LPUART2_CTS I2C1_SCL	ADC21 SEG21 TK21

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				**Alternate functions**	**Additional functions**
				I2C2_SCL	
				TIM1_CH1N	
				TIM2_CH1_ETR	
				EVENTOUT	
				PVD_OUT	
				TIM3_CH3	
				WKUP2	
21	PC11	I/O	COM	SPI1_NSS/I2S1_WS	ADC22 SEG22 TK22
				SPI2_MOSI/I2S2_SD	
				USART2_RX	
				USART2_TX	
				LPUART2_RTS_DE	
				TIM1_CH2N	
				TIM3_CH4	
				TIM3_ETR	
22	PC12	I/O	COM_F	USART2_CK	ADC6 SEG23 TK23
				LPUART1_RX	
				SPI1_NSS/I2S1_WS	
				UART2_RX	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA TIM1_CH1 TIM3_CH3 PWM_CH3 TIM3_ETR	
23	PC13	I/O	COM_F	USART2_TX UART2_TX LPUART2_TX I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA TIM1_CH2 TIM2_CH3 TIM17_BRK PWM_CH4 EVENTOUT PVD_OUT	ADC7 SEG24 TK24
24	PC14	I/O	COM_F	SPI1_NSS/I2S1_WS I2C1_SCL/I2C1_SDA	ADC8 SEG25

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				I2C2_SCL/I2C2_SDA TIM1_CH3 TIM2_CH4 TIM15_BRK EVENTOUT	TK25
25	PC15	I/O	COM_F	SPI1_SCK/I2S1_CK I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA TIM1_CH4 TIM2_ETR TIM15_CH1 PWM_CH2	ADC9 SEG26 COMP1_INP2 TK26
26	PD0	I/O	COM	SPI1_NSS/I2S1_WS USART1_CK UART1_TX UART1_RX TIM1_CH3N TIM15_CH1N PWM_CH2N	ADC10 SEG27 COMP1_INP3 TK27

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				MCO	
27	PD1	I/O	COM	SPI1_SCK/I2S1_CK USART1_TX UART1_TX UART1_RX TIM2_ETR TIM3_ETR PWM_CH1	ADC11 SEG28 COMP1_INP4 OPA_OUT2 TK28
28	PD2	I/O	COM	SPI1_MISO/I2S1_MCK USART1_RX USART1_TX UART2_RX UART2_TX LPUART2_CTS TIM1_CH2 TIM2_CH1 TIM3_CH1 TIM15_BRK	ADC12 SEG29 OPA_INM1 TK29
29	PD3	I/O	COM	SPI1_MOSI/I2S1_SD	ADC13

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				USART1_RX	SEG30/VLD0 OPA_INP1 TK30
				USART1_TX	
				UART2_RX	
				UART2_TX	
				LPUART2_RTS_DE	
				TIM1_CH2N	
				TIM2_CH2	
				TIM3_CH2	
				PWM_ETR	
				EVENTOUT	
30	PD4	I/O	COM	USART1_CK	ADC14 SEG31/VLCD1 OPA_OUT1 TK31
				TIM1_CH1N	
				TIM1_ETR	
				PWM_CH1N	
				EVENTOUT	
				WKUP3	
31	PD5	I/O	COM_F	SPI2_NSS/I2S2_WS	SEG32/VLCD2
				USART1_RX	
				LPUART2_RX	

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				I2C1_SMBA PWM_BRK LPTIM1_OUT_IN1	
32	PD6	I/O	COM_F	SPI2_SCK/I2S2_CK USART1_TX LPUART2_TX I2C1_SCL I2C2_SCL TIM1_CH3N LPTIM2_OUT_IN1 EVENTOUT	SEG33/VLCD3
33	PD7	I/O	COM_F	SPI1_MOSI/I2S1_SD SPI2_MOSI/I2S2_SD USART2_RX I2C1_SDA I2C2_SDA TIM15_CH1_ETR EVENTOUT	ADC15 SEG34/VLCDH
34	PD8-BOOT0(4)	I/O	COM	SPI2_MISO/I2S2_MCK	ADC16

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
				USART2_TX TIM2_CH1_ETR TIM3_CH1	
35	PD9	I/O	COM_F	USART2_RX I2C2_SMBA TIM3_CH2 TIM15_CH1N EVENTOUT	ADC23 SEG35
36	PD10	I/O	COM_FT	USART1_RX USART2_TX UART2_RX LPUART1_CTS LPUART2_RX TIM17_CH1N I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA PWM_CH2 LPTIM2_IN2 EVENTOUT	-

Packages	Reset	Port type	Port structure	Functions	
LQFP64 R2				Alternate functions	Additional functions
37	PD11	I/O	COM_FT	USART1_TX UART2_TX LPUART1_RTS_DE LPUART2_TX I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA TIM3_CH3 TIM17_CH1 PWM_CH2N	-
38	PD12	I/O	COM_F	USART2_RX COMP1_OUT TIM3_CH4 I2C2_SMBA TIM17_CH1	ADC24

1. Configured by option bytes to choose PD13 or NRST.
2. After reset, when the option byte is configured to 0/0 (default state), PA5 and PA4 are configured as SWCLK and SWDIO.
3. PA4, PA5, PB6, and PB5 can be configured via options to select GPIO functionality or SWC/SWD functionality. Internal pull-up resistors for PA4 and PB6, and internal pull-down resistors for PA5 and PB5 are activated.

option[1:0]	PA5	PA4	PB6	PB5
0/0(default)	SWCLK	SWDIO	GPIO	GPIO
0/1	GPIO	GPIO	SWDIO	SWCLK
1/0	SWCLK	GPIO	SWDIO	GPIO
1/1	GPIO	SWDIO	GPIO	SWCLK

4. PD8-BOOT0 defaults to digital input mode and pull-down is enabled.
5. PA6, PA7 and PA8 in V_{BKP} domain are powered via a current-limited switch (3 mA sourcing). GPIO from PA6 to PA8 output mode restrictions:
    1) Maximum rate 2 MHz, load ≤30 pF.
    2) Cannot be used as current sources (e.g., LED driving).
6. When only V_{BAT} is powered, PA6,PA7,PA8 in V_{BKP} domain may be in one of the following states: analog mode, input mode, push-pull with pull-up, or push-pull with pull-down.

    Design recommendations:

    1) Add a 1 to 10 MΩ resistor to ground on PA6,PA7,PA8 to prevent leakage current when the pin is in input mode.
    2) Resistor selection (as in recommendation 1) should account for the output current when the pin is configured as push-pull with pull-up.
7. PA0 requires 1 µF external capacitor when using V_{REFBUF}. ADC/DAC cannot use V_{REFBUF} as reference if PA0 is not routed.
8. Pins configured for SWD/SWC functions cannot be used as TK channels.

3.2. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TIM1_CH3	LPTIM1_OUT_IN1	-	-	-	-	-	-	-	-	USART2_TX	COMP2_OUT	-	-	-
PA1	TIM1_CH4	LPTIM2_OUT_IN1	TIM16_BRK	-	-	-	-	-	-	-	TIM1_CH3N	TIM2_ETR	-	-	-	-
PA2	TIM15_CH2	TIM15_CH1_ETR	TIM15_BRK	-	-	-	-	-	-	-	-	SPI1_NSS/ I2S1_WS	-	-	-	-
PA3	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	SPI1_SCK/ I2S1_CK	-	-	-	-
PA4	DEBUG_SWD	-	-	-	-	-	-	-	-	-	-	-	-	-	IR_OUT	
PA5	DEBUG_SWC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA6	TIM1_BRK	-	-	-	-	-	-	-	TIM15_CH1	-	USART1_CTS	USART1_TX	TIM2_CH4	-	-	EVENTOUT
PA7	-	-	-	-	-	-	-	-	TIM1_CH1	-	-	-	-	-	-	EVENTOUT
PA8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA9	TIM15_ETR	USART1_TX	USART1_RX	-	-	-	-	-	TIM15_CH1	-	-	-	-	-	-	EVENTOUT
PA10	USART1_TX	USART1_RX	-	-	-	-	-	-	TIM15_CH2	-	-	-	-	-	-	-
PA13	-	PWM_CH1	I2C1_SCL	I2C2_SCL	-	-	-	-	-	-	USART1_RTS	-	TIM1_BRK	-	-	EVENTOUT
PA14	MCO	PWM_CH1N	I2C1_SDA	I2C2_SDA	-	-	-	-	-	COMP2_OUT	USART2_CTS	USART2_RX	TIM15_CH1	-	-	EVENTOUT
PA15	TIM16_CH1	UART1_TX	UART1_RX	I2C1_SMBA	-	-	-	PWM_CH3	-	-	USART2_RTS	USART2_TX	TIM15_CH2	-	-	-

3.3. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	TIM16_CH1N	UART1_TX	UART1_RX	I2C2_SMBA	-	-	-	PWM_CH4	-	-	USART2_CK	SPI2_NSS/I2S2_WS	PWM_CH3	-	PVD_OUT	EVENTOUT
PB1	TIM2_CH3	TIM2_CH1_ETR	TIM16_BRK	-	-	-	-	-	-	-	-	SPI2_SCK/I2S2_CK	PWM_CH4	-	-	EVENTOUT
PB2	-	-	LPTIM1_OUT_IN1	LPUART1_TX	-	-	-	-	-		-	SPI2_MISO/I2S2_MCK	TIM15_ETR	-	-	EVENTOUT
PB3	-	-	LPTIM2_OUT	LPUART1_TX	SPI2_NSS/I2S2_WS	-	-	-	-	TIM2_CH2	-	SPI2_MOSI/I2S2_SD	LPTIM2_IN1	-	-	EVENTOUT
PB4	-	-	TIM2_CH3	SPI2_SCK/I2S2_CK	I2C1_SCL	-	I2C2_SCL	-	-	-	-	TIM1_BRK	-	-	-	EVENTOUT
PB5	DEBUG_SWC	-	TIM2_CH4	SPI2_MOSI/I2S2_SD	I2C1_SDA	-	I2C2_SDA	-	-	-	-	UART1_RX	-	-	-	-
PB6	DEBUG_SWD	-	TIM1_CH3	TIM2_ETR	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-	UART1_TX	-	-	-	EVENTOUT
PB7	-	-	-	TIM1_CH4	TIM1_ETR	SPI1_MISO/I2S1_MCK	SPI1_NSS/I2S1_WS	-	-	-	-	-	-	-	-	EVENTOUT
PB8	-	-	-	TIM1_CH4	TIM2_ETR	SPI1_MOSI/I2S1_SD	I2C1_SDA	-	I2C2_SDA	-	USART2_CTS	UART1_RX	LPUART1_RX	-	-	EVENTOUT
PB9	MCO	-	TIM2_CH4	TIM1_BRK	SPI1_SCK/I2S1_CK	I2C2_SCL	-	I2C2_SCL	USART2_TX/USART2_7816_IO	COMP1_OUT	USART2_RTS	UART1_TX	LPUART1_TX	PWM_BRK	LPTIM1_ETR	IR_OUT
PB10	-	TIM15_CH1_ETR	SPI1_NSS/I2S1_WS	-	LPTIM2_IN2	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB11	-	TIM2_CH1_ETR	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-	LPUART1_CTS	USART1_RX	-	-	-	-
PB12	-	TIM1_CH1	USART2_TX	SPI2_SCK/I2S2_CK	SPI1_MISO/I2S1_MCK	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	LPUART1_RTS_DE	USART1_TX	-	TIM17_CH1	LPTIM1_ETR	-
PB13	MCO	TIM1_CH1N	USART2_RX	SPI2_MOSI/I2S2_SD	SPI1_MOSI/I2S1_SD	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	UART2_RX	UART1_RX	LPUART1_RX	TIM17_CH1N	LPTIM2_ETR	EVENTOUT
PB14	-	TIM1_CH1	USART2_TX	SPI2_MISO/I2S2_MCK	LPTIM2_IN2	-	-	-	-	-	UART2_TX	UART1_TX	LPUART1_TX	TIM17_BRK	RTC_REFIN	EVENTOUT
PB15	-	TIM2_CH1_ETR	SPI2_NSS/I2S_WS	-	-	-	-	-	-	-	USART2_CK	TIM3_CH3	-	-	-	EVENTOUT

3.4. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-5 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	TIM15_CH1_ETR	PWM_BRK	TIM2_CH3	-	-	-	-	-	-	USART2_TX/USART2_7816_IO	TIM3_CH4	-	-	-	EVENTOUT
PC1	-	PWM_CH1	SPI1_NSS/I2S1_WS	-	-	-	-	-	-	-	-	CAN_RX	-	USART2_CTS	-	-
PC2	PWM_CH1N	SPI1_SCK/I2S1_CK	-	-	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-	CAN_TX	-	TIM15_CH1N	-	-
PC3	LPTIM2_OUT_IN1	TIM15_CH1	UART1_TX	UART1_RX	SPI1_MISO/I2S1_MCK	-	-	-	UART2_TX	UART2_RX	USART1_CTS	SPI2_NSS/I2S2_WS	LPTIM1_IN2	PWM_CH2N	TIM1_CH4	-
PC4	LPTIM1_OUT_IN1	TIM16_CH1	UART2_TX	UART2_RX	SPI1_MOSI/I2S1_SD	-	-	-	UART2_TX	UART2_RX	USART1_RTS	SPI2_SCK/I2S2_CK	LPTIM1_IN2	TIM1_CH3N	PWM_ETR_HS	-
PC5	TIM_CH3	TIM1_ETR	LPUART1_TX	LPUART1_RX	SPI2_SCK/I2S2_CK	I2C1_SCL	-	-	I2C1_SCL	-	-	LPTIM1_IN1	-	USART1_CTS	-	EVENTOUT
PC6	TIM3_CH4	LPTIM1_OUT_IN1	LPUART1_TX	LPUART1_RX	SPI2_MOSI/I2S2_SD	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	TIM1_CH3N	-	LPUART2_RX	USART1_RTS	UART2_RX	EVENTOUT
PC7	TIM15_ETR	TIM16_CH1N	LPUART1_TX	SPI2_MISO/I2S2_MCK	I2C1_SDA	-	-	I2C2_SDA	-	-	-	-	LPUART2_TX	USART2_TX/USART2_7816_IO	UART2_TX	EVENTOUT
PC8	TIM15_CH2	LPTIM2_OUT_IN1	TIM1_BRK	USART1_TX	USART1_RX	SPI1_MISO/I2S1_MCK	CAN_RX	-	-	-	-	-	UART1_RX	-	-	EVENTOUT
PC9	TIM15_CH1	TIM15_ETR	USART1_TX	USART1_RX	SPI1_MOSI/I2S1_SD	I2C1_SDA	CAN_TX	I2C2_SDA		-	USART2_CK	-	UART1_TX	-	LPTIM2_ETR	EVENTOUT
PC10	-	TIM3_CH3	TIM2_CH1_ETR	USART2_TX	USART2_RX	SPI1_SCK/I2S1_CK	I2C1_SCL		I2C2_SCL	-	LPUART2_CTS	-	TIM1_CH1N	-	PVD_OUT	EVENTOUT
PC11	-	TIM3_CH4	TIM3_ETR	USART2_TX	USART2_RX	SPI1_NSS/I2S1_WS	-	-	-	-	LPUART2_RTS_DE	SPI2_MOSI/I2S2_SD	TIM1_CH2N	-	-	-
PC12	-	TIM3_CH3	TIM3_ETR	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	-	UART2_RX	USART2_CK	LPUART1_RX	TIM1_CH1	SPI1_NSS/I2S1_WS	PWM_CH3	-
PC13	-	TIM2_CH3	TIM17_BRK	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	-	UART2_TX	USART2_TX/USART2_RX/USART2_7816_IO	LPUART2_TX	TIM1_CH2	PVD_OUT	PWM_CH4	EVENTOUT
PC14	-	TIM2_CH4	TIM15_BRK	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	-	-	-	SPI1_NSS/I2S1_WS	TIM1_CH3	-	-	EVENTOUT
PC15	-	TIM2_ETR	TIM15_CH1	I2C1_SCL	I2C1_SDA	-	I2C2_SCL	I2C2_SDA	-	PWM_CH2	-	SPI1_SCK/I2S1_CK	TIM1_CH4	-	-	-

3.5. Alternate functions selected through GPIOD_AFR registers for port D

Table 3-6 Port D alternate function mapping

PortD	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	MCO	TIM15_CH1N	UART1_TX	UART1_RX	-	-	-	-	-	PWM_CH2N	USART1_CK	SPI1_NSS/I2S1_WS	TIM1_CH3N	-	-	-
PD1	-	TIM3_ETR	PWM_CH1	UART1_TX	UART1_RX	-	-	-	-	-	UART1_TX/USART1_RX/USART2_7816_IO	SPI1_SCK/I2S1_CK	TIM2_ETR	-	-	-
PD2	-	TIM3_CH1	TIM15_BRK	USART1_TX	USART1_RX	-	-	-	-	TIM1_CH2N	LPUART2_CTS	SPI1_MISO/I2S1_MCK	TIM2_CH1	UART2_TX	UART2_RX	-
PD3	-	TIM3_CH2	PWM_ETR	USART1_TX	USART1_RX	-	-	-	-	TIM1_CH2N	LPUART2_RTS_DE	SPI1_MOSI/I2S1_SD	TIM2_CH2	UART2_TX	UART2_RX	EVETNOUT
PD4	-	TIM1_CH1N	PWM_CH1N	-	-	-	-	-	-	-	USART1_CK	-	TIM1_ETR	-	-	EVETNOUT
PD5	PWM_BRK	SPI2_NSS/I2S2_WS	-	I2C1_SMBA	-	-	-	-	LPTIM1_OUT_IN1			USART1_RX	LPUART2_RX	-	-	-
PD6	SPI2_SCK/I2S2_CK	I2C1_SCL	I2C2_SCL	-	-	-	-	-	LPTIM2_OUT_IN1	TIM1_CH3N	-	USART1_TX	LPUART2_TX	-	-	EVETNOUT
PD7	TIM15_CH1_ETR	USART2_RX	SPI2_MOSI/I2S2_SD	I2C1_SDA	I2C2_SDA	-	-	-	-	-	-	-	SPI1_MOSI/I2S1_SD	-	-	EVETNOUT
PD8	TIM2_CH1_ETR	USART2_TX	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-	-	-	TIM3_CH1	-	-	-	-
PD9	-	TIM15_CH1N	USART2_RX	-	-	-	-	-	-	-	-	TIM3_CH2	-	I2C2_SMBA	-	EVETNOUT
PD10	-	TIM17_CH1N	USART2_TX	-	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	UART2_RX	PWM_CH2	LPUART1_CTS	USART1_RX	LPUART2_RX	-	LPTIM2_IN2	EVETNOUT
PD11	-	PWM_CH2N	-	-	I2C1_SCL	I2C1_SDA	I2C1_SCL	I2C1_SDA	UART2_TX	-	LPUART1_RTS_DE	USART1_TX	LPUART2_TX	TIM3_CH3	TIM17_CH1	-
PD12	-	TIM17_CH1	-	I2C2_SMBA	-	-	-	-	-	-	-	USART2_RX	COMP1_OUT	TIM3_CH4	-	-
PD13	-	-	-	-	-	-	-	-	-	-	-	USART1_CK	TIM2_CH3	-	-	-

4. Memory mapping

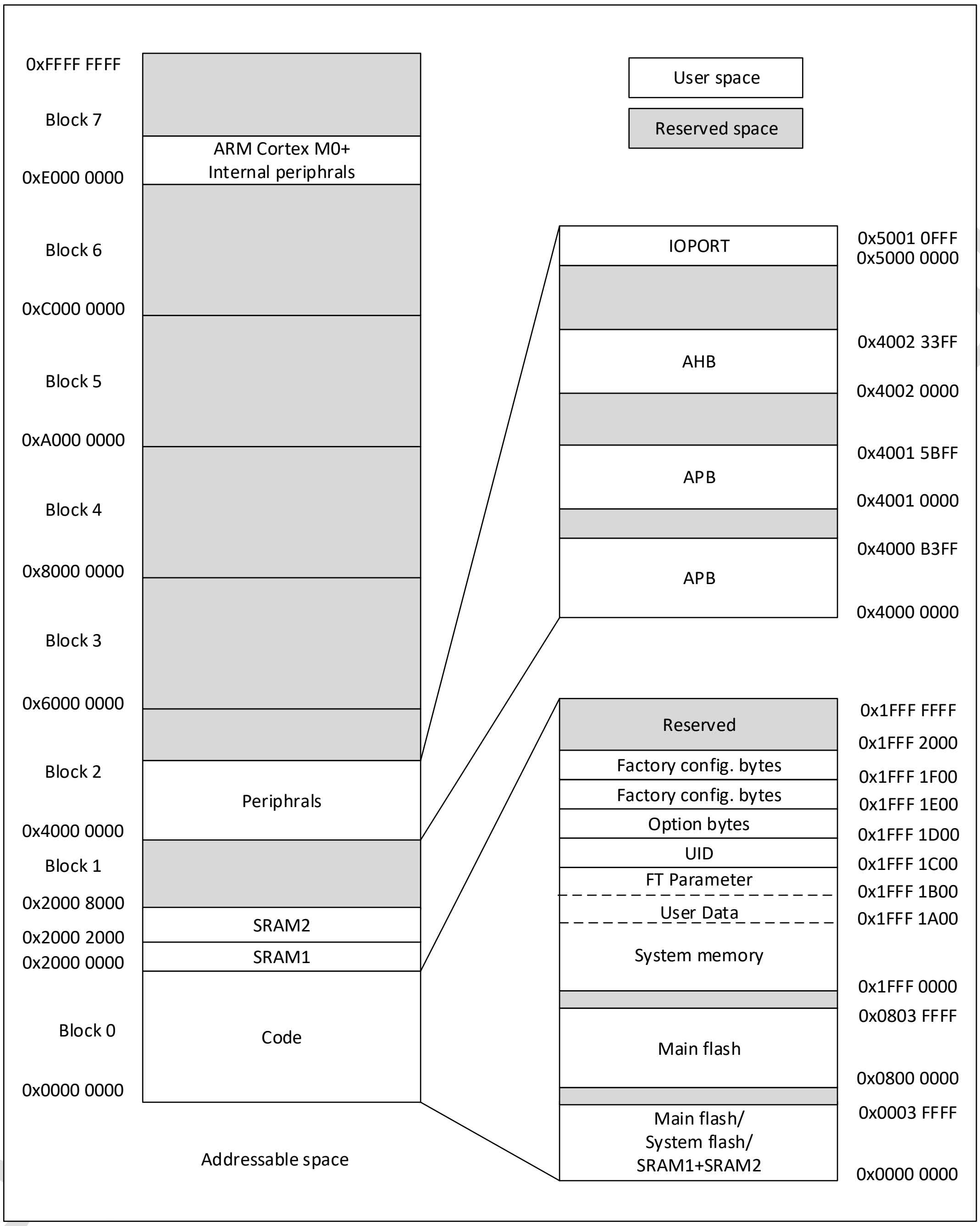


Figure 4-1 Memory map

Table 4-1 Memory boundary address

Type	Boundary address	Size	Memory area	Description
SRAM	0x2000 8000-0x3FFF FFFF	-	Reserved	-
	0x2000 2000-0x2000 7FFF	24 KB	SRAM2	SRAM address space: 0x20000000–0x20001FFF when configured to 8 KB on power-on.
	0x2000 0000-0x2000 1FFF	8 KB	SRAM1	
Code	0x1FFF 2000-0x1FFF FFFF	-	Reserved	-
	0x1FFF 1F00-0x1FFF 1FFF	256 bytes	Factory config. bytes	Store trimming data
	0x1FFF 1E00-0x1FFF 1EFF	256 bytes	Factory config. bytes	HSI trimming data, Flash erase/write time configuration parameters, TS data storage.
	0x1FFF 1D00-0x1FFF 1DFF	256 bytes	Option bytes	Option bytes information
	0x1FFF 1C00-0x1FFF 1CFF	256 bytes	UID	Unique ID
	0x1FFF 1B00-0x1FFF 1BFF	256 bytes	FT	FT info
	0x1FFF 1A00-0x1FFF 1AFF	256 bytes	User data bytes	User OTP
	0x1FFF 0000-0x1FFF 19FF	6.5 KB	System memory	Store Boot loader
	0x0804 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0803 FFFF	256 KB	Main flash memory	-
	0x0004 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0003 FFFF	256 KB	Selection based on Boot configuration： 1) Main flash memory 2) System flash memory 3) SRAM	-

Table 4-2 Peripheral register address

Bus	Boundary address	Size	Peripheral
	0xE000 0000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved
	0x5000 1400-0x5000 17FF	-	Reserved
	0x5000 1000-0x5000 13FF	-	Reserved
	0x5000 0C00-0x5000 0FFF	1 KB	GPIOD
	0x5000 0800-0x5000 0BFF	1 KB	GPIOC
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 3000-0x4002 33FF	1 KB	CRC

Bus	Boundary address	Size	Peripheral
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash
	0x4002 1800-0x4002 1FFF	2 KB	Reserved
	0x4002 1400-0x4002 17FF	1 KB	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 0400-0x4002 0FFF	-	Reserved
	0x4002 0000-0x4002 03FF	1 KB	DMA
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5800-0x4001 5BFF	-	MCUDBG
	0x4001 5000-0x4001 57FF	-	Reserved
	0x4001 4C00-0x4001 4FFF	1 KB	PWM
	0x4001 4800-0x4001 4BFF	1 KB	TIM17
	0x4001 4400-0x4001 47FF	1 KB	TIM16
	0x4001 4000-0x4001 43FF	1 KB	TIM15
	0x4001 3C00-0x4001 3FFF	-	Reserved
	0x4001 3800-0x4001 3BFF	1 KB	USART1
	0x4001 3400-0x4001 37FF	1 KB	Reserved
	0x4001 3000-0x4001 33FF	1 KB	SPI1
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 2800-0x4001 2BFF	1 KB	TK
	0x4001 2400-0x4001 27FF	1 KB	ADC
	0x4001 0C00-0x4001 23FF	-	Reserved
	0x4001 0800-0x4001 0BFF	1KB	V_{REFBUF}
	0x4001 0400-0x4001 07FF	1 KB	EXTI
	0x4001 0300-0x4001 03FF	1 KB	OPA
	0x4001 0200-0x4001 02FF		COMP1/COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	-	Reserved
	0x4000 B000-0x4000 B3FF	1 KB	BKP(TAMP)
	0x4000 9C00-0x4000 AFFF	-	Reserved
	0x4000 9800-0x4000 9BFF	1 KB	LPUART2
	0x4000 9400-0x4000 97FF	1 KB	LPTIM2
	0x4000 8400-0x4000 93FF	4 KB	Reserved
	0x4000 8000-0x4000 83FF	1KB	LPUART1
	0x4000 7C00-0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800-0x4000 7BFF	-	Reserved
	0x4000 7400-0x4000 77FF	1 KB	DAC
	0x4000 7000-0x4000 73FF	1 KB	PWR

Bus	Boundary address	Size	Peripheral
	0x4000 6800-0x4000 6FFF	1 KB	Reserved
	0x4000 6400-0x4000 67FF	1KB	CAN
	0x4000 5C00-0x4000 63FF	-	Reserved
	0x4000 5800-0x4000 5BFF	1 KB	I^2C2
	0x4000 5400-0x4000 57FF	1 KB	I^2C1
	0x4000 5000-0x4000 53FF	-	Reserved
	0x4000 4C00-0x4000 4FFF	1KB	UART2
	0x4000 4800-0x4000 4BFF	1KB	UART1
	0x4000 4400-0x4000 47FF	1 KB	USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	SPI2
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 2800-0x4000 2BFF	1 KB	RTC
	0x4000 2400-0x4000 27FF	1 KB	LCD
	0x4000 1800-0x4000 23FF	-	Reserved
	0x4000 1400-0x4000 17FF	1 KB	TIM7
	0x4000 1000-0x4000 13FF	1 KB	TIM6
	0x4000 0800-0x4000 0FFF	-	Reserved
	0x4000 0400-0x4000 07FF	1 KB	TIM3
	0x4000 0000-0x4000 03FF	1 KB	TIM2

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

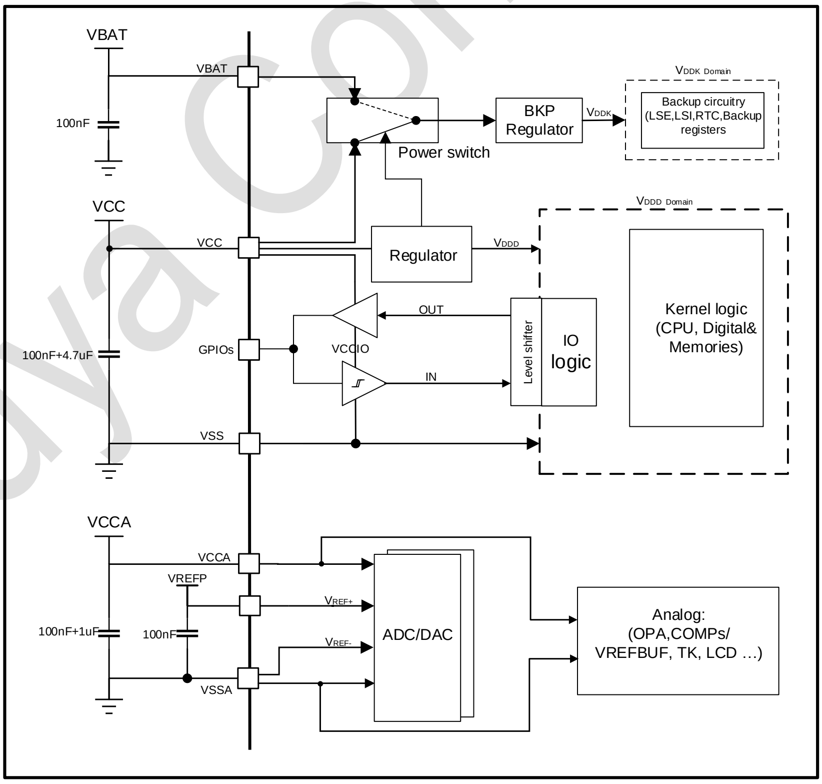
Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range). Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated.

5.1.3. Power supply scheme



Note: All decoupling capacitors need to be as close as possible to the pins on the PCB.

Figure 5-1 Power supply scheme

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{CC}–V_{SS}(1)	External mains power supply	-0.3	6.25	V
V_{IN}(2)	Input voltage on Tolerant IO(COM_T,COM_FT)	-0.3	6.25	V
	Input voltage on any other pins	-0.3	V_{CC}+0.3	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. Maximum V_{IN} must always follow allowable maximum injection current limits as per the table.

Table 5-2 Current characteristics

Symbol	Ratings	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	210	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	190	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	200	
	Total output current sourced by sum of all I/Os and control pins	180	
I_{IO}(2)	Output current sunk by any I/O and control pin except COM_L I/O	60	
	Output current sunk by any COM_L I/O	140	
	Output current source by any I/O and control pin(3)	25	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.
3. Excluding PA6/PA7/PA8 in V_{BKP} domain , which are powered via a current-limited switch (3 mA sourcing).

Table 5-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_O	Operating temperature range	-40 to +105	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB clock frequency	-	0	72	MHz
V_{CC}	Standard operating voltage	-	1.8	5.5	V
V_{BAT}	Backup operating voltage	-	1.55	5.5	V
V_{REFP}	ADC/DAC reference voltage	-	1.8	5.5	V
V_{IN}	Input voltage on Tolerant IO (COM_T, COM_FT)	-	-0.3	5.5	V
	Input voltage on any other pins	-	-0.3	V_{CC}+0.3	

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	110	℃

5.3.2. Operating conditions at power-on/power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise time rate	-	10	∞	µs/V
	V_{CC} fall time rate	V_{CC} and V_{BAT} drop synchronously	20	∞	
		V_{CC} drop and V_{BAT} remain stable	200	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 POR/PDR/BOR module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.55(2)	1.63	1.74	V
		Falling edge	1.5	1.58	1.7 (2)	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	20	-	mV
V_{BOR}	BOR threshold	BOR_LEV[2:0]=000 (Rising edge)	1.65(2)	1.75	1.84	V
		BOR_LEV[2:0]=000 (Falling edge)	1.56	1.65	1.74(2)	
		BOR_LEV[2:0]=001 (Rising edge)	1.84(2)	1.95	2.06	
		BOR_LEV[2:0]=001 (Falling edge)	1.75	1.85	1.96(2)	
		BOR_LEV[2:0]=010 (Rising edge)	2.02(2)	2.14	2.26	
		BOR_LEV[2:0]=010 (Falling edge)	1.93	2.04	2.15(2)	
		BOR_LEV[2:0]=011 (Rising edge)	2.21(2)	2.34	2.46	
		BOR_LEV[2:0]=011 (Falling edge)	2.11	2.23	2.36(2)	
		BOR_LEV[2:0]=100 (Rising edge)	2.59(2)	2.74	2.89	
		BOR_LEV[2:0]=100 (Falling edge)	2.48	2.62	2.77(2)	
		BOR_LEV[2:0]=101 (Rising edge)	2.87(2)	3.04	3.2	
		BOR_LEV[2:0]=101 (Falling edge)	2.76	2.92	3.08(2)	
		BOR_LEV[2:0]=110 (Rising edge)	3.4(2)	3.6	3.8	
		BOR_LEV[2:0]=110 (Falling edge)	3.33	3.52	3.72(2)	
		BOR_LEV[2:0]=111 (Rising edge)	3.88(2)	4.11	4.34	
		BOR_LEV[2:0]=111 (Falling edge)	3.78	4	4.22(2)	
$V_{\_BOR\_hyst}$(2)	BOR hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-7 PVD module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	PVD threshold	PLS[2:0]=000 (Rising edge)	1.65(1)	1.75	1.84	V
		PLS[2:0]=000 (Falling edge)	1.56	1.65	1.74(1)	
		PLS[2:0]=001 (Rising edge)	1.84(1)	1.95	2.06	
		PLS[2:0]=001 (Falling edge)	1.75	1.85	1.96(1)	
		PLS[2:0]=010 (Rising edge)	2.02(1)	2.14	2.26	
		PLS[2:0]=010 (Falling edge)	1.93	2.04	2.15(1)	
		PLS[2:0]=011 (Rising edge)	2.21(1)	2.34	2.46	
		PLS[2:0]=011 (Falling edge)	2.11	2.23	2.36(1)	
		PLS[2:0]=100 (Rising edge)	2.59(1)	2.74	2.89	
		PLS[2:0]=100 (Falling edge)	2.48	2.62	2.77(1)	
		PLS[2:0]=101 (Rising edge)	2.87(1)	3.04	3.2	
		PLS[2:0]=101 (Falling edge)	2.76	2.92	3.08(1)	
		PLS[2:0]=110 (Rising edge)	3.4(1)	3.6	3.8	
		PLS[2:0]=110 (Falling edge)	3.33	3.52	3.72(1)	
		PLS[2:0]=111 (Rising edge)	3.88(1)	4.11	4.34	
		PLS[2:0]=111 (Falling edge)	3.78	4	4.22(1)	
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV

1. Data based on characterization results, not tested in production.

5.3.4. Supply current characteristics

Table 5-8 Current consumption in Run mode

Sym-bol	Conditions						Typ[1]	Max		Unit
	Run	Code	Peripheral	System clock	Frequency (MHz)	MR_VSEL	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{CC} (Run)	Flash	While(1)	All peripherals enable	PLL[2]	72	2’b00	10.57	10.72	10.84	mA
					64	2’b00	9.45	9.65	9.77	
					48	2’b00	7.20	7.36	7.48	
				HSI	64	2’b00	9.23	9.37	9.46	
					48	2’b00	6.98	7.18	7.28	
					24	2’b00	3.66	3.80	3.94	
					16	2’b00	2.53	2.67	2.83	
					8	2’b10	1.25	1.35	1.49	
				LSI(FLASH_LPCR.SLEEP_EN=0)	32.768 kHz	2’b10	0.20	0.33	0.48	
				LSI(FLASH_LPCR.SLEEP_EN=1)	32.768 kHz	2’b10	0.14	0.27	0.42	
			All peripherals disable	PLL[2]	72	2’b00	5.01	5.26	5.39	
					64	2’b00	4.50	4.66	4.78	
					48	2’b00	3.47	3.68	3.82	
				HSI	64	2’b00	4.45	4.63	4.75	
					48	2’b00	3.36	3.55	3.68	
					24	2’b00	1.85	2.04	2.21	
					16	2’b00	1.30	1.50	1.68	
					8	2’b10	0.71	0.84	0.99	
				LSI(FLASH_LPCR.SLEEP_EN=0)	32.768 kHz	2’b10	0.18	0.33	0.48	
				LSI(FLASH_LPCR.SLEEP_EN=1)	32.768 kHz	2’b10	0.13	0.27	0.42	

1. Data based on characterization results, not tested in production.
2. HSI 8M is the reference clock source of PLL.

Table 5-9 Current consumption in Low-power run mode

Sym-bol	Conditions						Typ(1)	Max		Unit
	Run	Code	Peripheral	System clock	Frequency (MHz)	LPR_VSEL	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{CC} (LPR)	Flash	While(1)	All peripherals enable	MSI	2	2’b00	0.49	0.67	0.87	mA
					1	2’b10	0.36	0.54	0.74	
					250 kHz	2’b10	0.26	0.45	0.64	
					62.5 kHz	2’b10	0.24	0.42	0.62	
			All peripherals disable	MSI	2	2’b00	0.35	0.53	0.72	
					1	2’b10	0.29	0.47	0.67	
					250 kHz	2’b10	0.25	0.43	0.62	
					62.5 kHz	2’b10	0.23	0.42	0.61	

1. Data based on characterization results, not tested in production.

Table 5-10 Current consumption in Sleep mode

Symbol	Conditions						Typ(1)	Max		Unit
	Run	Code	Peripheral	System clock	Frequency (MHz)	MR_VSEL	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{CC} (Sleep)	Flash	While(1)	All peripherals enable	PLL(2)	72	2'b00	8.08	8.45	8.57	mA
					64	2'b00	7.23	7.56	7.69	
					48	2'b00	5.51	5.80	5.93	
				HSI	64	2'b00	7.05	7.35	7.46	
					48	2'b00	5.35	5.62	5.74	
					24	2'b00	2.83	3.04	3.20	
					16	2'b00	1.97	2.17	2.34	
					8	2'b10	0.99	1.14	1.28	
				LSI	32.768 kHz	2'b10	0.18	0.33	0.48	
			All peripherals disable	PLL(2)	72	2'b00	2.15	2.34	2.51	
					64	2'b00	1.94	2.14	2.31	
					48	2'b00	1.54	1.73	1.91	
				HSI	64	2'b00	1.91	2.10	2.27	
					48	2'b00	1.49	1.68	1.86	
					24	2'b00	0.90	1.09	1.28	
					16	2'b00	0.68	0.87	1.06	
					8	2'b10	0.42	0.58	0.73	
				LSI	32.768 kHz	2'b10	0.18	0.33	0.48	

1. Data based on characterization results, not tested in production.
2. HSI 8M is the reference clock source of PLL.

Table 5-11 Current consumption in Low-power sleep mode

Symbol	Conditions						Typ[1]	Max		Unit
	Run	Code	Peripheral	System clock	Frequency (MHz)	LPR_VSEL	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{CC} (LPS)	Flash	While(1)	All peripherals enable	MSI	2	2’b00	0.43	0.64	0.80	mA
					1	2’b10	0.33	0.51	0.70	
					250 kHz	2’b10	0.25	0.45	0.62	
					62.5 kHz	2’b10	0.23	0.41	0.60	
			All peripherals disable	MSI	2	2’b00	0.27	0.50	0.69	
					1	2’b10	0.25	0.44	0.64	
					250 kHz	2’b10	0.23	0.41	0.60	
					62.5 kHz	2’b10	0.22	0.41	0.59	

1. Data based on characterization results, not tested in production.

Table 5-12 Current consumption in Stop0 mode

Symbol	**Conditions**		**Typ(1)**	**Max**		**Unit**
	-	**LPR_VSEL/DLPR_VSEL**	**T_A = 25 ℃**	**T_A = 85 ℃**	**T_A = 105 ℃**	
I_{CC}(Stop0)	RTC + IWDG + LPTIM with LSI	LPR_VSEL = 2’b11	40.29	198.62	332.24	μA
	IWDG with LSI	LPR_VSEL = 2’b11	39.99	198.21	332.41	
	LPTIM with LSI	LPR_VSEL = 2’b11	40.18	198.45	332.35	
	RTC with LSI	LPR_VSEL = 2’b11	40.13	198.33	332.30	
	Peripheral l shutdown	LPR_VSEL = 2’b11	39.78	197.98	332.63	
	RTC + IWDG + LPTIM with LSI	DLPR_VSEL = 2’b00	13.10	165.93	334.98	
	IWDG with LSI	DLPR_VSEL = 2’b01	10.39	126.54	272.83	
	LPTIM with LSI	DLPR_VSEL = 2’b01	10.50	126.75	273.11	
	RTC with LSI	DLPR_VSEL = 2’b01	10.46	126.69	273.02	
	Peripheral l shutdown	DLPR_VSEL = 2’b01	10.12	126.33	272.67	

1. Data based on characterization results, not tested in production.

Table 5-13 Current consumption in Stop1 mode

Symbol	**Conditions**		**Typ[1]**	**Max**		**Unit**
	-	**LPR_VSEL/DLPR_VSEL**	**T_A = 25 ℃**	**T_A = 85 ℃**	**T_A = 105 ℃**	
I_{CC}(Stop1)	RTC + IWDG + LPTIM with LSI	LPR_VSEL = 2’b11	38.22	152.05	288.99	µA
	IWDG with LSI	LPR_VSEL = 2’b11	37.97	151.70	288.61	
	LPTIM with LSI	LPR_VSEL = 2’b11	38.10	151.95	288.94	
	RTC with LSI	LPR_VSEL = 2’b11	38.04	151.84	288.68	
	Peripheral shutdown	LPR_VSEL = 2’b11	37.70	151.56	288.47	
	RTC + IWDG + LPTIM with LSI	DLPR_VSEL = 2’b00	12.43	122.87	260.90	
	IWDG with LSI	DLPR_VSEL = 2’b01	7.73	91.18	196.01	
	LPTIM with LSI	DLPR_VSEL = 2’b01	7.84	91.38	196.34	
	RTC with LSI	DLPR_VSEL = 2’b01	7.81	91.33	196.26	
	Peripheral shutdown	DLPR_VSEL = 2’b01	7.50	90.97	195.96	

1. Data based on characterization results, not tested in production.

Table 5-14 Current consumption in Stop2 mode

Symbol	**Conditions**		**Typ**[(1)]	**Max**		**Unit**
	-	**LPR_VSEL/DLPR_VSEL**	**T_A = 25 ℃**	**T_A = 85 ℃**	**T_A = 105 ℃**	
I_{CC}(Stop2)	RTC + IWDG + LPTIM with LSI	LPR_VSEL = 2’b11	36.28	142.68	266.08	μA
	IWDG with LSI	LPR_VSEL = 2’b11	36.04	142.29	265.44	
	LPTIM with LSI	LPR_VSEL = 2’b11	36.19	142.53	265.90	
	RTC with LSI	LPR_VSEL = 2’b11	36.11	142.46	265.79	
	Peripheral shutdown	LPR_VSEL = 2’b11	35.54	142.09	265.29	
	RTC + IWDG + LPTIM with LSI	DLPR_VSEL = 2’b00	10.34	113.20	235.20	
	IWDG with LSI	DLPR_VSEL = 2’b01	7.44	87.46	183.81	
	LPTIM with LSI	DLPR_VSEL = 2’b01	7.54	87.65	184.04	
	RTC with LSI	DLPR_VSEL = 2’b01	7.51	87.60	183.95	
	Peripheral shutdown	DLPR_VSEL = 2’b01	7.22	87.26	184.42	

1. Data based on characterization results, not tested in production.

Table 5-15 Current consumption in Stop3 mode

Symbol	**Conditions**		**Typ(1)**	**Max**		**Unit**
	-	**LPR_VSEL/DLPR_VSEL**	**T_A = 25 ℃**	**T_A = 85 ℃**	**T_A = 105 ℃**	
I_{CC}(Stop3)	RTC + IWDG + LPTIM with LSI	LPR_VSEL = 2’b11	34.23	97.51	171.72	μA
	IWDG with LSI	LPR_VSEL = 2’b11	33.99	97.18	171.19	
	LPTIM with LSI	LPR_VSEL = 2’b11	34.14	97.36	171.55	
	RTC with LSI	LPR_VSEL = 2’b11	34.07	97.30	171.44	
	Peripheral shutdown	LPR_VSEL = 2’b11	33.67	96.98	171.04	
	RTC + IWDG + LPTIM with LSI	DLPR_VSEL = 2’b00	6.62	67.45	140.68	
	IWDG with LSI	DLPR_VSEL = 2’b01	4.74	52.03	109.86	
	LPTIM with LSI	DLPR_VSEL = 2’b01	4.84	52.22	110.08	
	RTC with LSI	DLPR_VSEL = 2’b01	4.81	52.17	110.00	
	Peripheral shutdown	DLPR_VSEL = 2’b01	4.52	51.83	110.20	

1. Data based on characterization results, not tested in production.

Table 5-16 Current consumption in Standby mode and V_{BAT}

Symbol	Conditions		Typ(1)	Max		Unit
	-	DLPR_VSEL	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{CC}(Standby)	RTC + IWDG with LSI	2’b01	3.13	27.75	57.33	μA
	IWDG with LSI	2’b01	3.06	27.64	57.20	
	RTC with LSI	2’b01	3.13	27.73	57.31	
	Peripheral shutdown	2’b01	1.88	14.41	30.45	
I_{VBAT}	RTC with LSI	-	1.68	4.79	8.40	
	Peripherall shutdown	-	1.40	4.47	8.03	

1. Data based on characterization results, not tested in production.

Table 5-17 Current consumption in TK mode

Symbol	Conditions					Typ(1)(2)	Max	Unit
	Mode	DLPR_VSEL	MR_VSEL	System clock	Frequency (MHz)			
I_{CC}(TK)	From Stop2 to Run mode	2’b01	2’b10	HSI	8	14.2	-	μA
	From Stop3 to Run mode	2’b01	2’b10		8	13.1	-	

1. Data based on characterization results, not tested in production.
2. Test in V_{CC} = 5 V,T_A = 25 ℃。

5.3.5. Wake-up time from low-power mode

Table 5-18 Wake-up time from low-power mode

Symbol	Parameter(1)	Power Supply (2)	Conditions	Typ(3)	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode to Run mode in Flash		-	10	-	CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode		-	10	-	
$t_{WULPRUN}$	Wake-up from Low-power run to Run mode in Flash	Regulator in LPR,LPR_VSEL = 00/10	HSI (8 MHz) as system clock	5	-	µs
t_{WUSTOP}(4)	Wake-up from Stop0 to Run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	HSI (8 MHz) as system clock	11	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	22	-	
	Wake-up from Stop1 to Run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	HSI (8 MHz) as system clock	11	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	22	-	
	Wake-up from Stop2 to Run mode in Flash	Regulator in LPR, LPR_VSEL = 00/01	HSI (8 MHz) as system clock	12	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	23	-	
	Wake-up from Stop3 to Run mode in Flash	Regulator in LPR, LPR_VSEL = 00/01	HSI (8 MHz) as system clock	12	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	23	-	
	Wake-up from Stop0 to Low-power run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	MSI (2 MHz) as system clock	22	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	MSI (2 MHz) as system clock	30	-	
	Wake-up from Stop1 to Low-power run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	MSI (2 MHz) as system clock	23	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	MSI (2 MHz) as system clock	31	-	
	Wake-up from Stop2 to Low-power run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	MSI (2 MHz) as system clock	31	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	MSI (2 MHz) as system clock	39	-	
	Wake-up from Stop3 to Low-power run mode in Flash	Regulator in LPR,LPR_VSEL = 00/01	MSI (2 MHz) as system clock	31	-	
		Regulator in DLPR,DLPR_VSEL = 00/01	MSI (2 MHz) as system clock	39	-	
t_{WUSTB}	Wake-up from Standby to Run mode in Flash(Load after power-on	Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	230	-	
	Wake-up from Standby to Run mode in Flash(no load after power-on)	Regulator in DLPR,DLPR_VSEL = 00/01	HSI (8 MHz) as system clock	25	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Power supply mode before wake-up.
3. Data based on characterization results, not tested in production.
4. PWR_CR1.HSION_CTRL = 1 'b1, PWR_CR1.FLS_SLPTIME = 2' b00 when Regulator in LPR.
   PWR_CR1.HSION_CTRL=1’b0, PWR_CR1.FLS_SLPTIME=2’b01 when Regulator in DLPR。

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

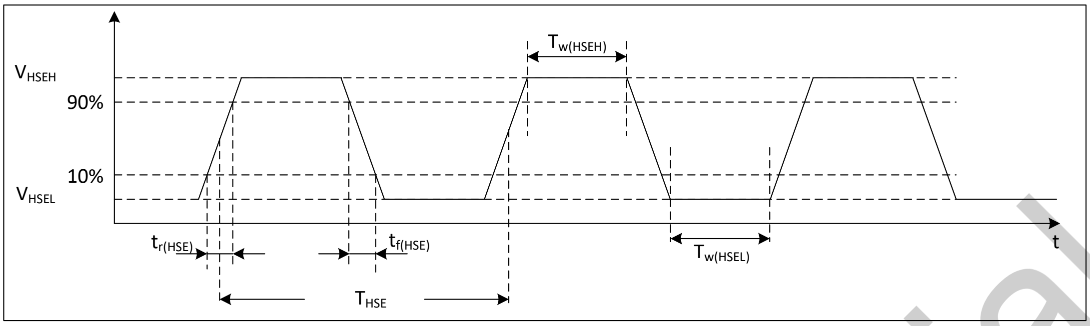


Figure 5-2 High-speed external clock timing diagram

Table 5-19 High-speed external clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	0.3*V_{CC}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the device stops working, and the corresponding I/O is used as a standard GPIO.

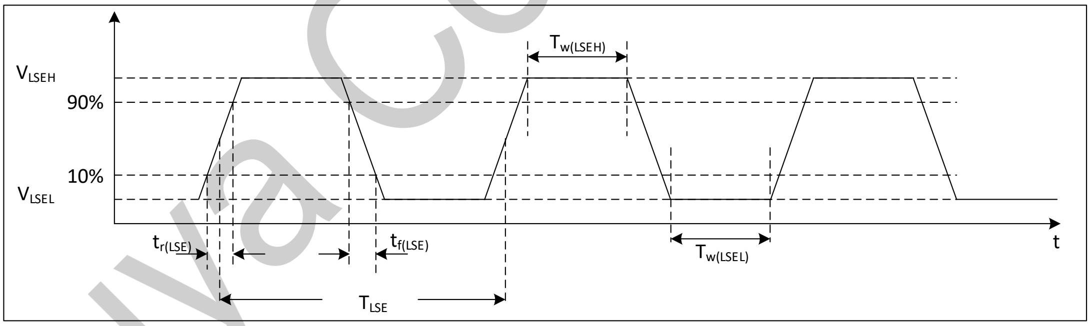


Figure 5-3 Low-speed external clock timing diagram

Table 5-20 Low-speed external clock characteristics(1)

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7 V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3 V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-21 HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
I_{CC}(4)	HSE current consumption	Startup time	-	-	5.5	mA
		V_{CC}=3.3 V,R_m=100 Ω, C_L=12 pF@4 MHz, HSE_DRV[1:0] = 00	-	0.5	-	
		V_{CC}=3.3 V,R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 00	-	0.59	-	
		V_{CC}=3.3 V,R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 01	-	1.1	-	
		V_{CC}=3.3 V,R_m=70 Ω, C_L=12 pF@16 MHz, HSE_DRV[1:0] = 01	-	1.28	-	
		V_{CC}=3.3 V,R_m=40 Ω, C_L=20 pF@24 MHz, HSE_DRV[1:0] = 10	-	1.55	-	
		V_{CC}=3.3 V,R_m=40 Ω, C_L=10 pF@32 MHz, HSE_DRV[1:0] = 10	-	1.46	-	
$t_{SU(HSE)}$(3) (4)	Startup time	V_{CC}=3.3 V,R_m=100 Ω, C_L=12 pF@4 MHz, HSE_DRV[1:0] = 00	-	2.6	-	ms
		V_{CC}=3.3 V,R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 00	-	6.04	-	
		V_{CC}=3.3 V,R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 01	-	1.54	-	
		V_{CC}=3.3 V,R_m=70 Ω, C_L=12 pF@16 MHz, HSE_DRV[1:0] = 01	-	1.8	-	
		V_{CC}=3.3 V,R_m=40 Ω, C_L=20pF@24 MHz, HSE_DRV[1:0] = 10	-	0.7	-	
		V_{CC}=3.3 V,R_m=40 Ω, C_L=10 pF@32 MHz, HSE_DRV[1:0] = 10	-	0.4	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.
4. Data based on characterization results, not tested in production.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-22 LSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{CC}(4)	LSE current consumption	C_L=6 pF, Rm=70 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 00	-	320	-	nA
		C_L=6 pF, Rm=70 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 01	-	520	-	
		C_L=12 pF, Rm=45 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 10	-	720	-	
		C_L=12 pF, Rm=45 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 11	-	1130	-	

Symbol	Parameter	Conditions$^{(1)}$	Min$^{(2)}$	Typ	Max$^{(2)}$	Unit
$t_{SU(LSE)}^{(3)(4)}$	Startup time	C_L=6 pF, Rm=70 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 00	-	1.3	-	s
		C_L=6 pF, Rm=70 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 01	-	0.6	-	
		C_L=12 pF, Rm=45 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 10	-	0.9	-	
		C_L=12 pF, Rm=45 kΩ LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 11	-	0.5	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-23 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	-	-	8.0 16.0 24.0 48.0 64.0	-	MHz
$\Delta_{Temp(HSI)}$	HSI 16/24/48 MHz frequency drift over temperature	V_{CC} = 3.3 V, T_A = 25 ℃	-1$^{(2)}$	-	1$^{(2)}$	%
		V_{CC} = 2.0 to 5.5 V, T_A = -20 to 85 ℃	-2$^{(2)}$	-	2$^{(2)}$	
		V_{CC} = 1.8 to 5.5 V, T_A = -40 to 105 ℃	-3$^{(2)}$	-	3$^{(2)}$	
	HSI 8/64 MHz frequency drift over temperature	V_{CC} = 3.3 V, T_A = 25 ℃	-1$^{(2)}$	-	1$^{(2)}$	
		V_{CC} = 2.0 to 5.5 V, T_A = -20 to 105 ℃	-2.5$^{(2)}$	-	2.5$^{(2)}$	
		V_{CC} = 1.8 to 5.5 V, T_A = - 40 to 105 ℃	-5$^{(2)}$	-	5$^{(2)}$	
$f_{TRIM}^{(1)}$	HSI trimming accuracy	-	-	0.1	-	%
$D_{HSI}^{(1)}$	Duty cycle	-	45$^{(1)}$	-	55$^{(1)}$	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	3	4$^{(1)}$	μs
$I_{CC(HSI)}^{(2)}$	HSI power consumption	8 MHz	-	108	-	μA
		16 MHz	-	164	-	
		24 MHz	-	221	-	
		48MHz	-	326	-	
		64MHz	-	436	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Medium-speed internal (MSI) RC oscillator

Table 5-24 MSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MSI}	MSI frequency	-	-	2.0	-	MHz
$\Delta_{Temp(MSI)}$	MSI frequency drift over temperature	V_{CC} = 3.3 V, T_A = 25 ℃	-1[2]	-	1(2)	%
		V_{CC} = 1.8 to 5.5 V, T_A = 0 to 85 ℃	-3(2)	-	3(2)	
		V_{CC} = 1.8 to 5.5 V, T_A = -40 to 105 ℃	-4.5(2)	-	4.5(2)	
f_{TRIM}(1)	MSI trimming accuracy	-	-	0.1	-	%
D_{MSI}(1)	Duty cycle	-	45(1)	-	55(1)	%
$t_{Stab(MSI)}$	MSI stabilization time	-	-	6	10(1)	μs
$I_{CC(MSI)}$(2)	MSI power consumption	2 MHz	-	26	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Low-speed internal (LSI) RC oscillator

Table 5-25 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	-	-	32.768	-	kHz
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	T_A= 25 °C, V_{CC}= 3.3 V	-3(2)		3(2)	%
		V_{CC}= 1.8 to 5.5 V, T_A= 0 to 85 °C	-4(2)	-	4(2)	
		V_{CC}= 1.8 to 5.5 V,T_A= -40 to 105 °C	-7(2)	-	7(2)	
f_{TRIM}(1)	LSI trimming accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$(1)	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$(1)	LSI power consumption	-	-	300	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.10. Phase locked loop (PLL) characteristics

Table 5-26 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A = 25 °C, V_{CC} = 3.3 V	8(1)	-	24(1)	MHz
f_{PLL_OUT}	PLL output clock	T_A = 25 °C, V_{CC} = 3.3 V	48(1)	-	72	MHz
t_{LOCK}	PLL lock time	f_{PLL_IN} = 24 MHz	-	20	40(1)	μs

1. Guaranteed by design, not tested in production.

5.3.11. Memory characteristics

Table 5-27 Memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.0	3.0	mA
	Page/sector/mass erase supply current	-	2.0	3.0	

1. Guaranteed by design, not tested in production.

Table 5-28 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = - 40 to 85 °C	100	kcycle

Symbol	Parameter	Conditions	Min(1)	Unit
		T_A = -85 to 105 °C	10	
t_{RET}	Data retention time	10 kcycle T_A = 55 °C	20	Year

1. Data based on characterization results, not tested in production.

5.3.12. EFT characteristics

Table 5-29 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

5.3.13. ESD & LU characteristics

Table 5-30 ESD & LU characteristics

Symbol	Parameter	Standards	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	Any other pins except Tolerant IO and V_{BKP} domain pins	8	kV
			Tolerant IO and PA6/PA7/PA8 pins in V_{BKP} domain	6	
$V_{ESD(CDM)}$	Static discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	-	1	kV
LU	Static Latch-up	JESD78E	-	200	mA

5.3.14. I/O port characteristics

Table 5-31 IO port characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage Tolerant I/O input low level		1.8 V≤V_{CC}≤ 5.5 V	-	-	0.3*V_{CC}	V
V_{IH}	High level input voltage Tolerant I/O input high level		1.8 V≤V_{CC}≤ 5.5 V	0.7*V_{CC}	-	-	V
V_{hys} (1)	Schmitt trigger hysteresis Tolerant I/O Schmitt trigger hysteresis		-	-	200	-	mV
I_{lkg} (2)	Input leakage current	Standard I/O	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1	μA
		Tolerant I/O	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1	
			V_{CC}≤V_{IN}≤V_{CC}+1 V(4)	-	-	3	
			V_{CC+}1 V≤V_{IN}≤5.5 V	-	-	1	
R_{PU} (3)	Internal pull-up resistor		V_{IN}= V_{SS}	30	50	70	kΩ
R_{PD} (3)	Internal pull-down resistor		V_{IN}= V_{CC}	30	50	70	kΩ
C_{IO}	Pin capacitance		-	-	5	-	pF
$t_{ns(EXTI)}$ (1)	Input filter width		ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$ (1)	I^2C input filter width		ENI=1, EIIC=1	100	145	300	ns

1. Guaranteed by design, not tested in production.
2. If there is reverse current pouring in adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be a real resistor in series with a switchable PMOS/NMOS.
4. The maximum value of V_{CC}+1 V should not exceed 5.5 V.

Table 5-32 Output voltage characteristics(3)

Symbol	Parameter(1)	Driver	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O	GPIOx_OSPEEDR=11	I_{OL} = 50 mA, V_{CC} ≥ 5 V	-	0.4	V
		GPIOx_OSPEEDR=11	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	

Symbol	Parameter[1]	Driver	Conditions	Min	Max	Unit
	pin(all I/Os except COM_L)	GPIOx_OSPEEDR=11	I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OL}[2]	Output low level voltage for an I/O pin(COM_L)	GPIOx_OSPEEDR=11	I_{OL} = 120 mA, $V_{CC} \geq 5$ V	-	0.6	
		GPIOx_OSPEEDR=10	I_{OL} = 100 mA, $V_{CC} \geq 5$ V	-	0.5	
		GPIOx_OSPEEDR=01	I_{OL}=80 mA, $V_{CC} \geq 5$ V	-	0.5	
		GPIOx_OSPEEDR=00	I_{OL}=60 mA, $V_{CC} \geq 5$ V	-	0.4	
V_{OH}[2][4]	Output low level voltage for an I/O pin	GPIOx_OSPEEDR=11	I_{OL} =16 mA, $V_{CC} \geq 3.3$ V	V_{CC}-0.6	-	
		GPIOx_OSPEEDR=11	I_{OL} = 8 mA, $V_{CC} \geq 2.7$ V	V_{CC}-0.4	-	
		GPIOx_OSPEEDR=11	I_{OL} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.
4. Excluding PA6/PA7/PA8 in V_{BKP} domain , which are powered via a current-limited switch (3 mA sourcing).

5.3.15. Constent current LED SEG driver characteristics

Table 5-33 Constent current LED SEG driver characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	3.3	-	5.5	V
I_{OH}	Constent current mode 1 current	V_{CC} = 3.3 V,V_{OH} = V_{CC}/3	-	9.7	-	mA
I_{OH}	Constent current mode 2 current	V_{CC} = 3.3 V,V_{OH} = V_{CC}/3	-	7.4	-	mA
I_{OH}	Constent current mode 3 current	V_{CC} = 3.3 V,V_{OH} = V_{CC}/3	-	5	-	mA
I_{OH}	Constent current mode 4 current	V_{CC} = 3.3 V,V_{OH} = V_{CC}/3	-	2.5	-	mA
$\lvert\triangle I\rvert/I$	Current accuracy (unified calibration)	Constant current source outputs 10 mA current: (I-10) /10 (V_{CC} = 3.3 V,T_A = +25 ℃)	-	-	±15	%

1. Data based on characterization results, not tested in production.

5.3.16. ADC characteristics

Table 5-34 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Analog power supply	-	1.8	-	5.5	V
V_{REFP}	Positive reference voltage	-	1.8	-	V_{CC}	V
V_{REFN}	Negative reference voltage	-	0			V
I_{CC}	V_{CC} pin current	f_{ADC} = 16 MHz	-	1	-	mA
		f_{ADC} = 32 MHz	-	1	-	
I_{REF}	V_{REF} pin voltage	f_{ADC} = 16 MHz	-	15	-	µA
		f_{ADC} = 32 MHz	-	30	-	
f_{ADC}	ADC clock frequency	1.8 V≤V_{CC}≤5.5 V	4	-	8	MHz
		2.5 V≤V_{CC}≤5.5 V	4	-	16	
		2.7 V≤V_{CC}≤5.5 V	4	-	32	
f_S[2]	Sampling rate	V_{CC}≥1.8 V	-	-	0.5	Msps
		V_{CC}≥2.5 V	-	-	1	
		V_{CC}≥2.7 V	-	-	2	
V_{AIN}	Conversion voltage range[3]	Single-ended mode	0	-	V_{REFP}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Differential mode	$-V_{REFP}$	-	V_{REFP}	
R_{AIN}(2)	External input impedance(4)	-	-	-	33	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1.2	kΩ
C_{ADC}(2)	Internal sampling and holding capacitor	-	-	2.5	3	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz		12		µs
		-		192		$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 16 MHz	0.156	-	40.03	µs
		-	2.5	-	640.5	$1/f_{ADC}$
t_{samp_setup}	Sampling time for internal channels	-	20	-	-	µs
t_{STAB}(2)	Power-on stabilization time	-	0	0	3	µs
t_{CONV}(2)	Total conversion time	f_{ADC} = 16 MHz	1	-	40.875	µs
		-		16 - 654		$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. For some package types, V_{REFP} can be internally connected to V_{CC}, and V_{REFN} can be internally connected to V_{SS}. For details, please refer to the pin definitions.
4. When using external triggering, an additional delay of $1/f_{PCLK2}$ is required.
    a) $R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$
    b) The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (referring to 12-bit resolution).

Table 5-35 R_{AIN} Max for f_{ADC} = 32 MHz(1)

Sampling period (T_S)	Sampling time (t_s)(ns)	Maximum value of R_{AIN} (Ω)	
		Fast channel	Slow channel
2.5	78.13	100	-
6.5	203.13	330	100
12.5	390.63	680	470
24.5	765.63	1500	1200
47.5	1484.38	2200	1800
92.5	2890.63	4700	3900
247.5	7734.38	12000	10000
640.5	20015.63	39000	33000

1. Guaranteed by design, not tested in production.

Table 5-36 ADC static characteristics(($V_{REF} = V_{CC}$)(1)(2)(3)

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
ET	Total unadjusted error	V_{REFP} = V_{CC} = 3.3 V, f_{ADC} ≤ 48 MHz, 12-bit resolution	Single-ended mode	-	±4.0	-	LSB
			Differential mode	-	±3.0	-	
EO	Offset error		Single-ended mode	-	±5.0	-	
			Differential mode	-	±4.0	-	
EG	Gain error		Single-ended mode	-	±2.0	-	
			Differential mode	-	±1.5	-	
ED	Differential linearity error		Single-ended mode	-	-1.0 ~ 2.5	-	
			Differential mode	-	-1.0 ~ 2.0	-	
EL	Integral linearity		Single-ended mode	-	±2.5	-	
			Differential mode	-	±5.0	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-37 ADC static characteristics($V_{REFP} = V_{REFBUF}$)(1)(2)(3)

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
ET	Total unadjusted error	V_{CC} = 3.3 V, V_{REFP}= V_{REFBUF} = 0.6 V, f_{ADC} ≤ 32 MHz, 12-bit resolution	Single-ended mode	-	±6.0	-	LSB
			Differential mode	-	±5.0	-	
EO	Offset error		Single-ended mode	-	±2.5	-	
			Differential mode	-	±1.0	-	
EG	Gain error		Single-ended mode	-	±3.0	-	
			Differential mode	-	±2.0	-	
ED	Differential linearity error		Single-ended mode	-	-1.0 ~ 3.6	-	
			Differential mode	-	-1.0 ~ 3.5	-	
EL	Integral linearity		Single-ended mode	-	±3.5	-	
			Differential mode	-	±3.5	-	
ET	Total unadjusted error	V_{CC} = 3.3 V, V_{REFP}= V_{REFBUF} = 1.024/1.5/2.048/2.5 V, f_{ADC} ≤ 32 MHz, 12-bit resolution	Single-ended mode	-	±3.0	-	
			Differential mode	-	±2.5	-	
EO	Offset error		Single-ended mode	-	±2.0	-	
			Differential mode	-	±2.0	-	
EG	Gain error		Single-ended mode	-	±1.5	-	
			Differential mode	-	±1.5	-	
ED	Differential linearity error		Single-ended mode	-	-1.0 ~ 2.5	-	
			Differential mode	-	-1.0 ~ 2.5	-	
EL	Integral linearity		Single-ended mode	-	±3.0	-	
			Differential mode	-	±3.0	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-38 ADC dynamic characteristics($V_{REFP} = V_{CC}$)(1)(2)(3)

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
ENOB	Effective number of bits	$V_{REFP} = V_{CC}$ = 3.3 V, f_{ADC} ≤ 48 MHz, 12-bit resolution	Single-ended mode	-	10.0	-	bit
			Differential mode	-	10.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	62.0	-	dB
			Differential mode	-	63.5	-	
SNR	Signal to noise ratio		Single-ended mode	-	62.3	-	
			Differential mode	-	63.7	-	
SFDR	Spurious free dynamic range		Single-ended mode	-	80.4	-	
			Differential mode	-	79.6	-	

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
THD	Total harmonic distortion		Single-ended mode	-	-73.9	-	
			Differential mode	-	-76.6	-	
ENOB	Effective number of bits	V_{REFP} = V_{CC} = 3.3 V, f_{ADC} ≤ 32 MHz , 12-bit resolution, Run in SRAM	Single-ended mode	-	11.0	-	bit
			Differential mode	-	11.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	68.1	-	dB
			Differential mode	-	67.0	-	
SNR	Signal to noise ratio		Single-ended mode	-	68.5	-	
			Differential mode	-	70.7	-	
SFDR	Spurious free dynamic range		Single-ended mode	-	83.6	-	
			Differential mode	-	81.7	-	
THD	Total harmonic distortion		Single-ended mode	-	-78.7	-	
			Differential mode	-	-77.4	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-39 ADC dynamic characteristics (V_{REFP} = V_{REFBUF}) (1)(2)(3)

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
ENOB	Effective number of bits	V_{CC} = 3.3 V, V_{REFP} = V_{REFBUF} = 0.6 V, f_{ADC} ≤ 32 MHz, 12-bit resolution	Single-ended mode	-	8.0	-	bit
			Differential mode	-	9.8	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	49.8	-	dB
			Differential mode	-	61.1	-	
SNR	Signal to noise ratio		Single-ended mode	-	49.8	-	
			Differential mode	-	61.1	-	
SFDR	Spurious free dynamic range		Single-ended mode	-	85.4	-	
			Differential mode	-	89.1	-	
THD	Total harmonic distortion		Single-ended mode	-	-81.2	-	
			Differential mode	-	-84.1	-	
ENOB	Effective number of bits	V_{CC} = 3.3 V, V_{REFP} = V_{REFBUF} = 1.024 V, f_{ADC} ≤ 32 MHz, 12-bit resolution	Single-ended mode	-	9.0	-	bit
			Differential mode	-	10.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	56.0	-	dB
			Differential mode	-	64.0	-	
SNR	Signal to noise ratio		Single-ended mode	-	56.0	-	
			Differential mode	-	64.1	-	
SFDR	Spurious free dynamic range		Single-ended mode	-	84.6	-	
			Differential mode	-	87.8	-	

Symbol	Parameter	Conditions	Mode	Min	Typ	Max	Unit
THD	Total harmonic distortion		Single-ended mode	-	-81.6	-	
			Differential mode	-	-81.3	-	
ENOB	Effective number of bits	V_{CC} = 3.3 V, V_{REFP} = V_{REFBUF} = 1.5/2.048/2.5 V, f_{ADC} ≤ 32 MHz, 12-bit resolution	Single-ended mode	-	9.3	-	bit
			Differential mode	-	10.7	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	57.7	-	dB
			Differential mode	-	66.5	-	
SNR	Signal to noise ratio		Single-ended mode	-	57.7	-	
			Differential mode	-	67.5	-	
SFDR	Spurious free dynamic range		Single-ended mode	-	83.6	-	
			Differential mode	-	74.2	-	
THD	Total harmonic distortion		Single-ended mode	-	-79.4	-	
			Differential mode	-	-73.0	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

5.3.17. DAC characteristics

Table 5-40 DAC characteristics (V_{REFP} = V_{CC})

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	DAC supply voltage	Buffer ON	2.2	-	5.5	V
	DAC supply voltage	Buffer OFF	2.2	-	5.5	
R_{LOAD}(1)	Resistive load with buffer ON	Load connected to V_{SS}	5	-	-	kΩ
		Load connected to V_{CC}	15	-	-	
R_{O}(1)	DAC output load	The minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ when the buffer is OFF.	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).	-	-	50	pF
DAC_OUT min(1)	Highest DAC_OUT voltage (Buffer OFF)	give the maximum output excursion of the DAC	0.2	-	-	V
DAC_OUT max(1)	Highest DAC_OUT voltage (Buffer OFF)		-	-	V_{CC}-0.2	V
DAC_OUT min(1)	Highest DAC_OUT voltage (Buffer OFF)	give the maximum output excursion of the DAC	-	0.5	-	mV
DAC_OUT max(1)	Highest DAC_OUT voltage (Buffer OFF)		-	-	V_{CC}-0.01	V
I_{CC}(1)	V_{CC}consumption (2)	With no load, middle code (0x800) on the inputs	-	-	900	µA
		With no load, worst code (0xF1C) at V_{CC} = 3.6 V in terms of DC consumption on the input	-	-	1200	
DNL(2)	Differential linearity error	Given for the DAC in 8 bits configuration	-	-	±1	LSB
		Given for the DAC in 12 bits configuration	-	-	±2	
INL(2)	Integral linearity error	Given for the DAC in 8 bits configuration	-	-	±1	LSB
		Given for the DAC in 12 bits configuration			±4	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Offset[2]	Offset error	Given for the DAC in 8 bits configuration	-	-	±3	LSB
		Given for the DAC in 12 bits configuration	-	-	±12	
Gain error[2]	Gain error	Given for the DAC in 12 bits configuration	-	-	±0.5	%
$t_{SETTLING}$[2]	Settling time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ Full scale: for a 10 bits input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1 LSB	-	4	10	µs
Update rate[2]	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}[2]	Wake-up time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ, Input code between lowest and highest possible ones.	-	6.5	10	µs
P_{SRR+}[1]	Power supply rejection ratio (to V_{CC}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-41 DAC characteristics (V_{REFP} = V_{REFBUF} = 2.5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	DAC supply voltage	Buffer ON	2.8	-	5.5	V
	DAC supply voltage	Buffer OFF	2.8	-	5.5	
R_{LOAD}[1]	Resistive load with buffer ON	Load connected to V_{SS}	5	-	-	kΩ
		Load connected to V_{CC}	15	-	-	
R_O[1]	DAC output load	The minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ when the buffer is OFF.	-	-	15	kΩ
C_{LOAD}[1]	Capacitive load	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).	-	-	50	pF
DAC_OUT min[1]	Highest DAC_OUT voltage (Buffer OFF)	give the maximum output excursion of the DAC	0.2	-	-	V
DAC_OUT max[1]	Highest DAC_OUT voltage (Buffer OFF)		-	-	V_{REFBUF} - 0.2	V
DAC_OUT min[1]	Highest DAC_OUT voltage (Buffer OFF)	give the maximum output excursion of the DAC	-	0.5	-	mV
DAC_OUT max[1]	Highest DAC_OUT voltage (Buffer OFF)		-	-	V_{REFBUF} - 0.01	V
I_{CC}[1]	V_{CC} consumption[2]	With no load, middle code (0x800) on the inputs	-	-	900	µA
		With no load, worst code (0xF1C) at V_{CC} = 3.6 V in terms of DC consumption on the input	-	-	1200	
DNL[2]	Differential linearity error	Given for the DAC in 8 bits configuration	-	±1	-	LSB
		Given for the DAC in 12 bits configuration	-	±4	-	
INL[2]	Integral linearity error	Given for the DAC in 8 bits configuration	-	±1	-	LSB
		Given for the DAC in 12 bits configuration	-	±4	-	
Offset[2]	Offset error	Given for the DAC in 8 bits configuration	-	-	±3	LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Given for the DAC in 12 bits configuration	-	-	±12	
Gain error[2]	Gain error	Given for the DAC in 12 bits configuration	-	-	±0.5	%
$t_{SETTLING}$[2]	Settling time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ Full scale: for a 10 bits input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	4	10	µs
Update rate[2]	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}[2]	Wake-up time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ, Input code between lowest and highest possible ones.	-	6.5	10	µs
P_{SRR+}[1]	Power supply rejection ratio (to V_{CC}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.18. Comparator characteristics

Table 5-42 Comparator characteristics[1]

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IN}	Input voltage range	-			0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode			-	-	5	µs
		Medium-speed mode			-	-	15	
t_D	Propagation delay	200 mV step 100 mV overdrive	High-speed mode	V_{CC} ≥ 1.8 V	-	50	2000	ns
				V_{CC} ≥ 2 V	-		200	
			Medium-speed mode	V_{CC} ≥ 1.8 V	-	1500	5000	
				V_{CC} ≥ 2 V	-		4000	
		>200 mV step 100 mV overdrive	High-speed mode	V_{CC} ≥ 1.8 V	-	-	2000	
				V_{CC} ≥ 2 V	-	-	300	
			Medium-speed mode	V_{CC} ≥ 1.8 V	-	-	5000	
				V_{CC} ≥ 2 V	-	-	4000	
V_{offset}	Offset voltage	-		-	-	±5	±10	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	-	0	-	mV
		With hysteresis		-	-	20	-	
I_{CC}	Consumption	Static	High-speed mode	-	-	250	-	µA
			Medium-speed mode	-	-	10	-	
		With 50 kHz and ±100 mv overdrive square signal	High-speed mode	-	-	250	-	
			Medium-speed mode	-	-	10	-	

1. Guaranteed by design, not tested in production.

5.3.19. Operational amplifier characteristics

Table 5-43 OPA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	2.5	-	5.5	V
V_{IN}	Input voltage	-	0	-	V_{CC}	V
V_{OUT}	Output voltage	$C_{LOAD} \leq 25$ pF, $R_{LOAD} \geq 5$ kΩ	0.2	-	V_{CC}-0.2	V
I_{LOAD}	Drive current	-	-	-	1.0	mA
R_{Load}	Resister load	-	5	-	-	kΩ
C_{LOAD}	Capacitive load	-	-	-	25	pF
t_{start}	Initialization time	$C_{LOAD} \leq 25$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	20	μs
V_{IO}	Input offset voltage	$C_{LOAD} \leq 25$ pF, $R_{LOAD} \geq 5$ kΩ Vcom=V_{CC}/2	-	±10	-	mV
PM	Phase margin	$C_{LOAD} \leq 25$ pF, $R_{LOAD} \geq 5$ kΩ Vcom=V_{CC}/2	-	80	-	Deg
UGBW	Unit gain band width	$C_{LOAD} \leq 25$ pF, $R_{LOAD} \geq 5$ kΩ Vcom=V_{CC}/2	-	10	-	MHz
SR	Slew rate	-	-	8	-	V/μs

5.3.20. Temperature sensor characteristics

Table 5-44 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	℃
Avg_Slope(1)	Average slope	1.9	2.5	3.5	mV/℃
V_{30}	Voltage at 30 ℃ (±5 ℃)	0.742	0.76	0.785	V
t_{START}(1)	Start up time	-	70	120	μs
t_{S_temp}(1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.21. LCD controller characteristics

Table 5-45 LCD controller characteristics

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
I_{LCD}(4)	LCD supply current	LCD operating current Internal resistance drive mode(1)	-	2.6	-	μA
		External resistance drive mode (2)	-	0.4	-	
		External capacitance drive mode(3)	-	0.5	-	
R_L(4)	Low drive resistance	Internal resistance drive mode	-	6.2	-	MΩ
R_H(4)	High drive resistance	Internal resistance drive mode	-	30	-	kΩ
C_{ext}	Capacitance of a single external capacitor	External capacitance drive mode	-	100	-	nF
V_{LCDH}	LCD adjustable highest level voltage	-	-	V_{CC}	-	V
V_{LCD3}	LCD highest level voltage	-	-	V_{LCDH}	-	
V_{LCD2}	LCD 3/4 level voltage	-	-	3/4 V_{LCDH}	-	
V_{LCD1}	LCD 2/4 level voltage	-	-	2/4 V_{LCDH}	-	
V_{LCD0}	LCD 1/4 level voltage	-	-	1/4 V_{LCDH}	-	

1. LCD enabled, V_{CC} = 3.3 V, 1/8 duty, 1/4 bias, scanning frequency is 256 Hz, all pixels activated, internal resistance voltage division mode, high drive time. FCCTL [2:0] = 101, no external LCD screen is connected.
2. LCD enabled, V_{CC} = 3.3 V, 1/8 duty, 1/4 bias, scanning frequency is 512 Hz, all pixels activated, external resistance voltage division mode, external single-section resistance is 100 kΩ, excluding external resistance current, no external LCD screen is connected.

3. LCD enabled, V_{CC} = 3.3 V, 1/8 duty, 1/4 bias, scanning frequency is 512 Hz, all pixels activated, external capacitance voltage division mode, number of times to drive external capacitor SWCAP_DRV_NUM [2:0] = 000, no external LCD screen is connected.
4. Guaranteed by design, not tested in production.

5.3.22. Embedded voltage reference characteristics

Table 5-46 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start\_vrefint}$	Start time of V_{REFINT}	-	10	15	µs
T_{coeff}	Temperature coefficient of V_{REFINT}	-	150(1)	-	ppm/℃
I_{vcc}	V_{REFINT} current consumption from V_{CC}	-	12	20	µA

1. Guaranteed by design, not tested in production.

Table 5-47 Internal voltage reference buffer (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF25}	2.5 V Internal reference voltage	T_A = 25 °C,V_{CC} = 3.3 V	2.455	2.5	2.545	V
V_{REF20}	2.048 V Internal reference voltage	T_A = 25 °C,V_{CC} = 3.3 V	2.011	2.048	2.085	V
V_{REF15}	1.5 V Internal reference voltage	T_A = 25 °C,V_{CC} = 3.3 V	1.473	1.5	1.527	V
$V_{REF1024}$	1.024 V Internal reference voltage	T_A = 25 °C,V_{CC} = 3.3 V	1.006	1.024	1.042	V
V_{REF06}	0.6 V Internal reference voltage	T_A = 25 °C,V_{CC} = 3.3 V	0.589	0.6	0.611	V
$T_{coeff\_V'REF\text{-}BUF}$(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C, V_{REFBUF}= 1.024/1.5/2.048/2.5 V	-	150	-	ppm/°C
		T_A = -40 to 105 °C, V_{REFBUF}= 0.6 V	-	300	-	
$t_{start\_VREFBUF}$	Start time of V_{REFBUF}	-	-	350	450	µs

1. Guaranteed by design, not tested in production.

5.3.23. COMP Internal voltage reference buffer characteristics(6-bit DAC)

Table 5-48 Internal voltage reference buffer (V_{REFCMP}) characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$\triangle V_{abs}$	Absolute deviation	-	-	±0.5	-	LSB

1. Guaranteed by design, not tested in production.

5.3.24. Timer characteristics

Table 5-49 Timer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	13.889	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 72 MHz	-	36	-	
$t_{COUNTER}$	16-bit counter internal clock period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	910	-	µs
	32-bit counter clock period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	-	s

Table 5-50 LPTIM1 characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	131072000	ms
/2	1	0.0610	262144000	
/4	2	0.1221	524288000	
/8	3	0.2441	1048576000	
/16	4	0.4883	2097152000	
/32	5	0.9766	4194304000	
/64	6	1.9531	8388608000	
/128	7	3.9063	16777216000	

Table 5-51 LPTIM2 characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	2000	ms
/2	1	0.0610	4000	
/4	2	0.1221	8000	
/8	3	0.2441	16000	
/16	4	0.4883	32000	
/32	5	0.9766	64000	
/64	6	1.9531	128000	
/128	7	3.9063	256000	

Table 5-52 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	500	ms
/8	1	0.244	1000	
/16	2	0.488	2000	
/32	3	0.976	4000	
/64	4	1.952	8000	
/128	5	3.904	16000	
/256	6 or 7	7.808	32000	

Table 5-53 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.25. Communication interfaces

5.3.25.1. I^{2}Cinterface characteristics

I^{2}C interface meets the requirements of the I^{2}C bus specification and user manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I^{2}C SDA and SCL pins have analog filtering, see table below.

Table 5-54 I^{2}C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.25.2. SPI characteristics

Table 5-55 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$2*T_{pclk}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*T_{pclk}$	-	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high level/low level time	Master mode, presc = 2	T_{pclk}-2	T_{pclk}+1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1	-	ns
		Slave mode	3	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	2	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	3*T_{pclk}	ns
$t_{dis(SO)}$	Data output disable time	Slave mode, presc = 2	2*T_{pclk}	-	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	0	20	ns
$t_{v(MO)}$		Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode	2	-	ns
$t_{h(MO)}$		Master mode	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

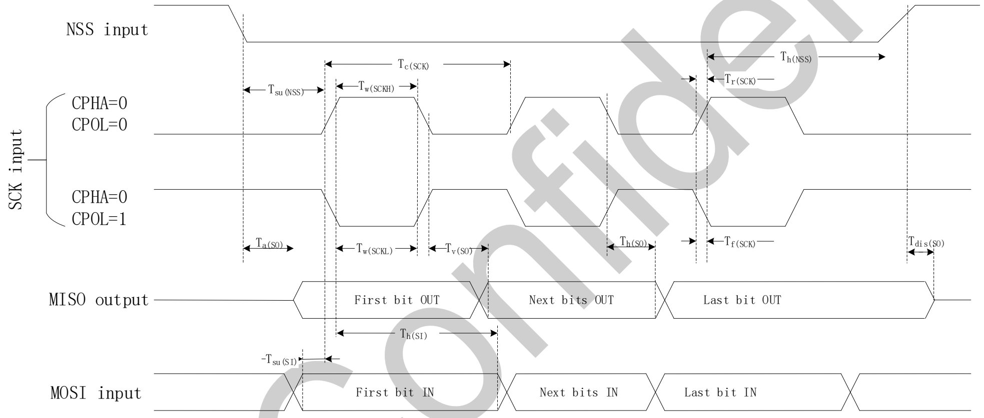


Figure 5-4 SPI timing diagram - Slave mode and CPHA=0

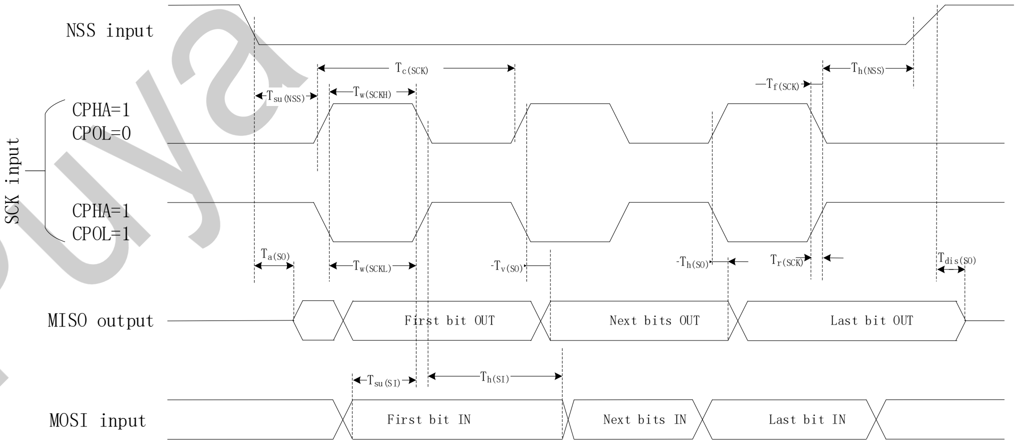


Figure 5-5 SPI timing diagram - Slave mode and CPHA=1

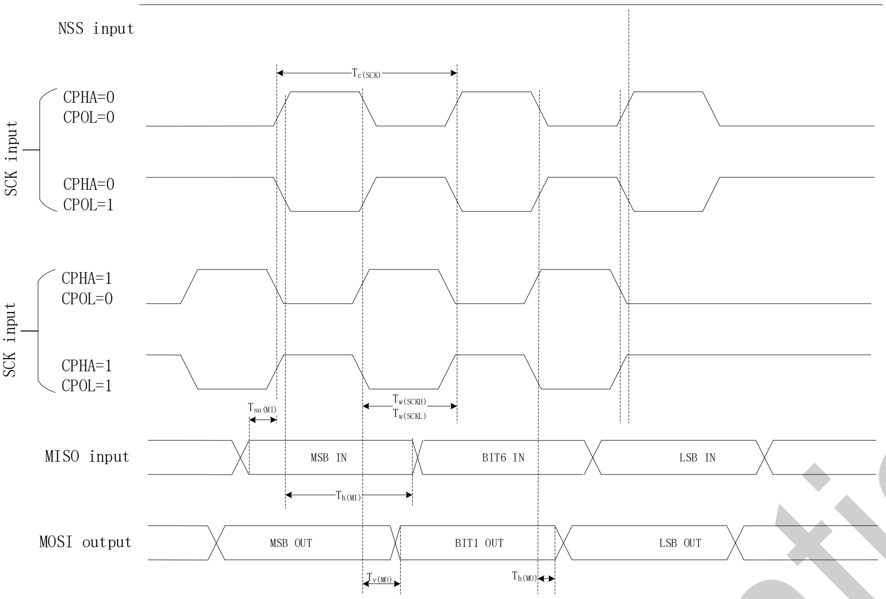


Figure 5-6 SPI timing diagram - Master mode

5.3.25.3. I^{2}S characteristics

Table 5-56 I^{2}S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_S	I^{2}S audio sampling frequency	-	8	192	kHz
f_{MCLK}	I^{2}S main clock output	-	256 x f_s	256 x f_s	kHz
f_{CK} $1/t_{c(CK)}$	I^{2}S clock frequency	Master mode	-	64 x f_s	kHz
		Slave mode	-	64 x f_s	
D_{CK}	I^{2}S clock duty cycle	Slave receiver	30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I^{2}S clock rise and fall time	Capacitive load:C_L = 50 pF	-	8	ns
$t_{v(WS)}$	W_S valid time	Master mode	-	2	
$t_{h(WS)}$	W_S hold time	Master mode	3	-	
		Slave mode	2	-	
$t_{su}(W_S)$	W_S setup time	Slave mode	4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master mode	3	-	
$t_{su(SD\_SR)}$		Slave mode	4	-	
$t_{h(SD\_MR)}$	Data input hold time	Master mode	5	-	
$t_{h(SD\_SR)}$		Slave mode	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave mode (after enable edge)	-	20	
$t_{v(SD\_MT)}$		Master mode (after enable edge)	-	5	
$t_{h(SD\_ST)}$	Data output hold time	Slave mode (after enable edge)	2	-	
$t_{h(SD\_MT)}$		Master mode (after enable edge)	1	-	

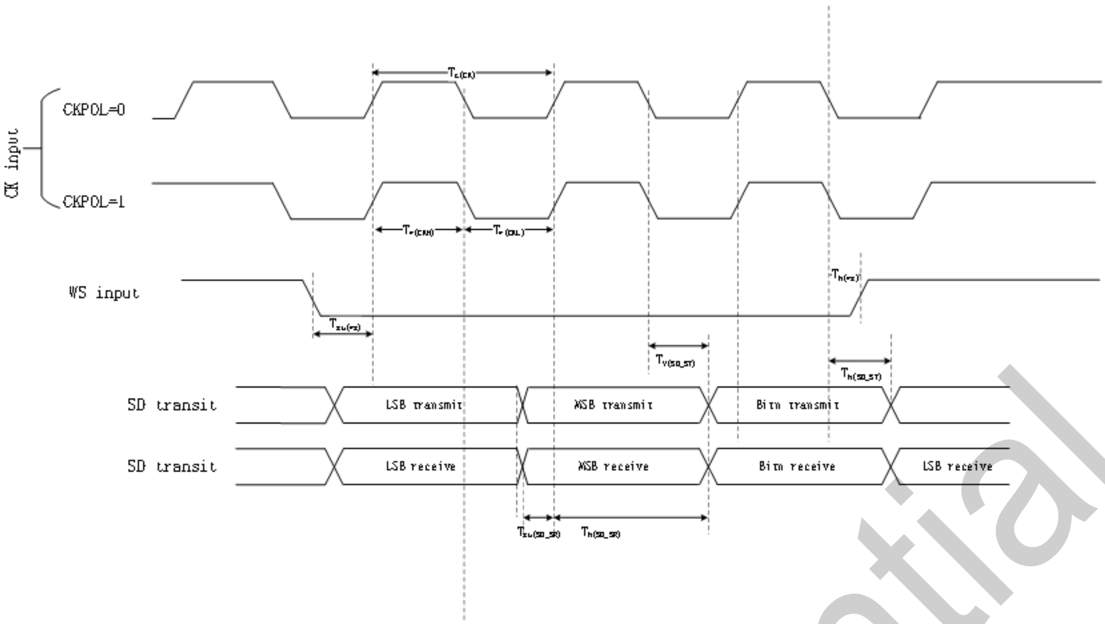


Figure 5-7 I^{2}S timing diagram-Slave mode(Philips protocol)

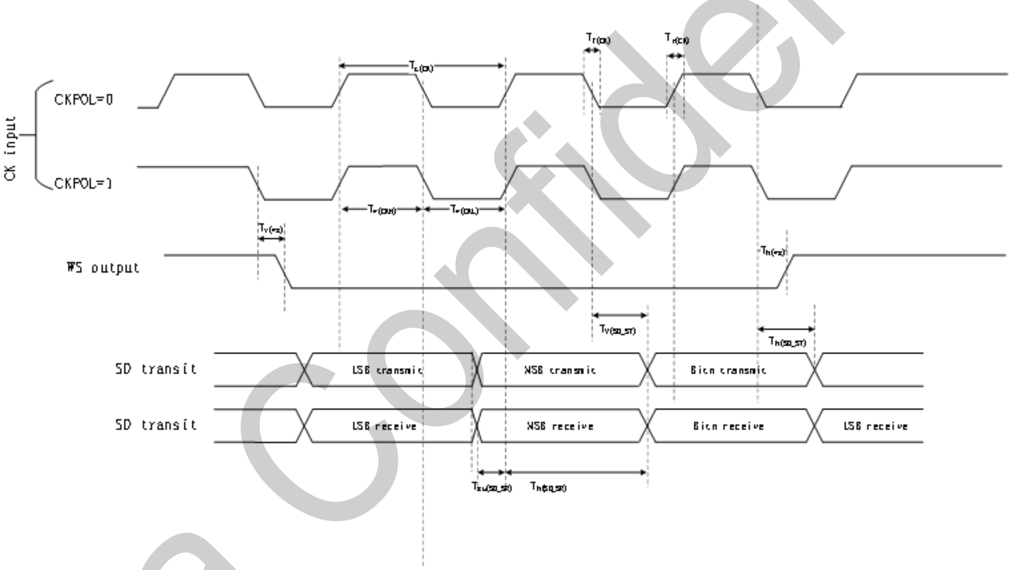


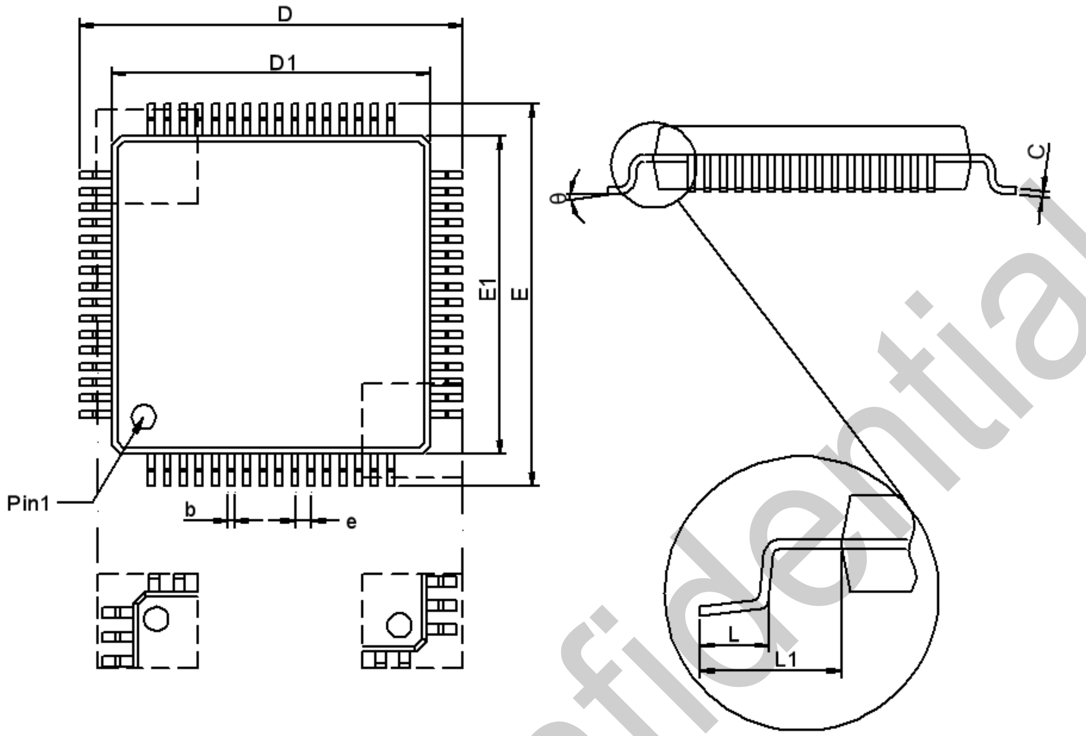
Figure 5-8 I^{2}S timing diagram-Master mode(Philips protocol)

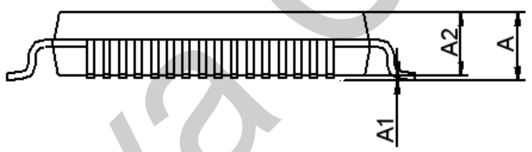
5.3.25.4. CAN characteristics

Refer to Section 5.3.14. I/O port characteristics for more details on the input/output alternate function characteristics.

6. Package information

6.1. LQFP64 package size





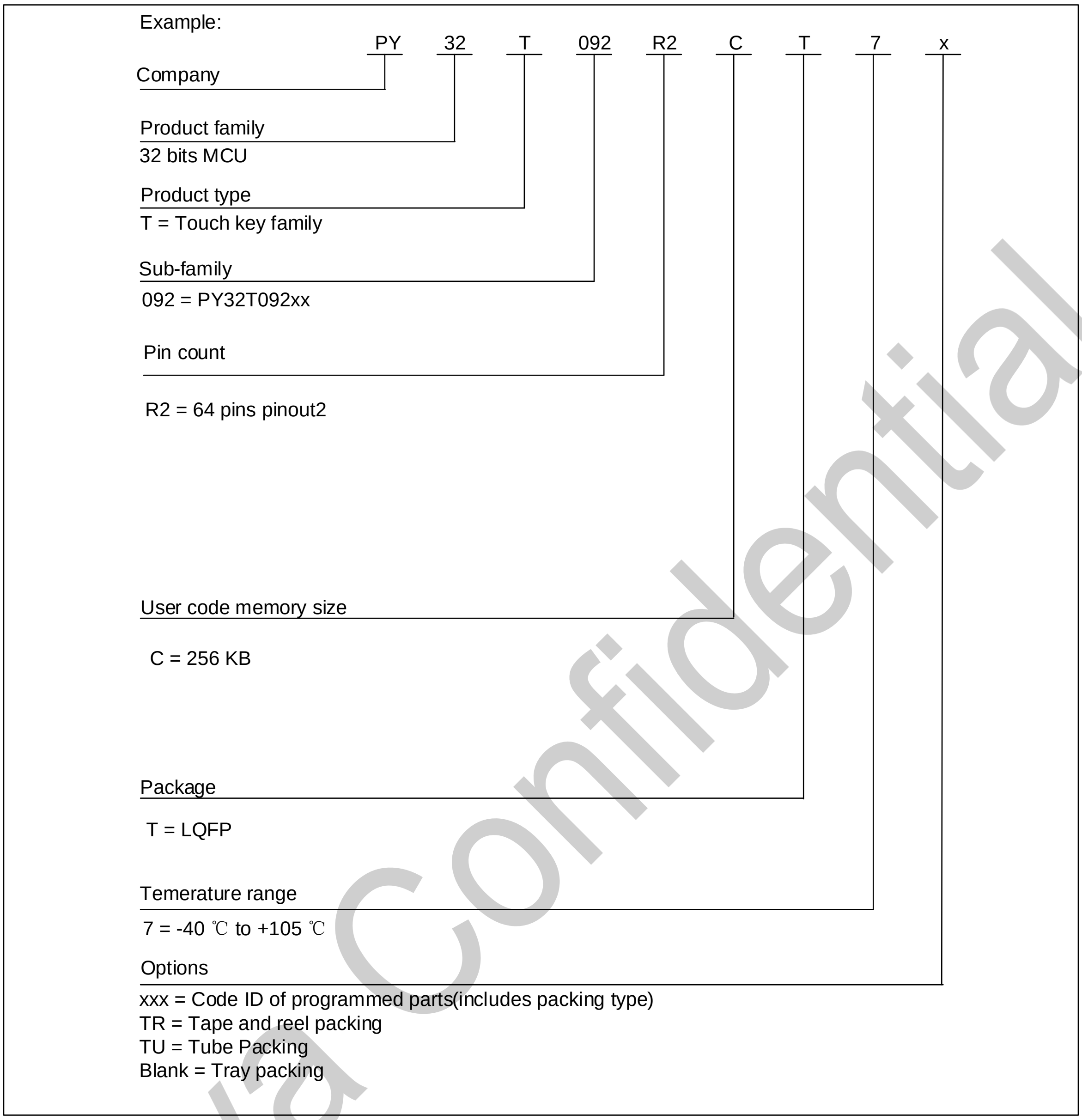
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	11.950	12.000	12.050
D1	9.900	10.000	10.100
E	11.950	12.000	12.050
E1	9.900	10.000	10.100
e		0.500BSC	
L	0.530	-	0.700
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE Puya LQFP64L 10x10X1.4-0.5PITCH	DRAWING NO. QRPD-0051	REV 1.1

7. Ordering information



Example:

PY 32 T 092 R2 C T 7 x

Company

Product family

32 bits MCU

Product type

T = Touch key family

Sub-family

092 = PY32T092xx

Pin count

R2 = 64 pins pinout2

User code memory size

C = 256 KB

Package

T = LQFP

Temerature range

7 = -40 ℃ to +105 ℃

Options

xxx = Code ID of programmed parts(includes packing type)
TR = Tape and reel packing
TU = Tube Packing
Blank = Tray packing

8. Version history

Version	Date	Description
V0.6	2025.04.03	Initial version
V0.7	2025.11.04	Update product version information and change PY32T092R2CT7 product definition.

Puya Semiconductor Co., Ltd.